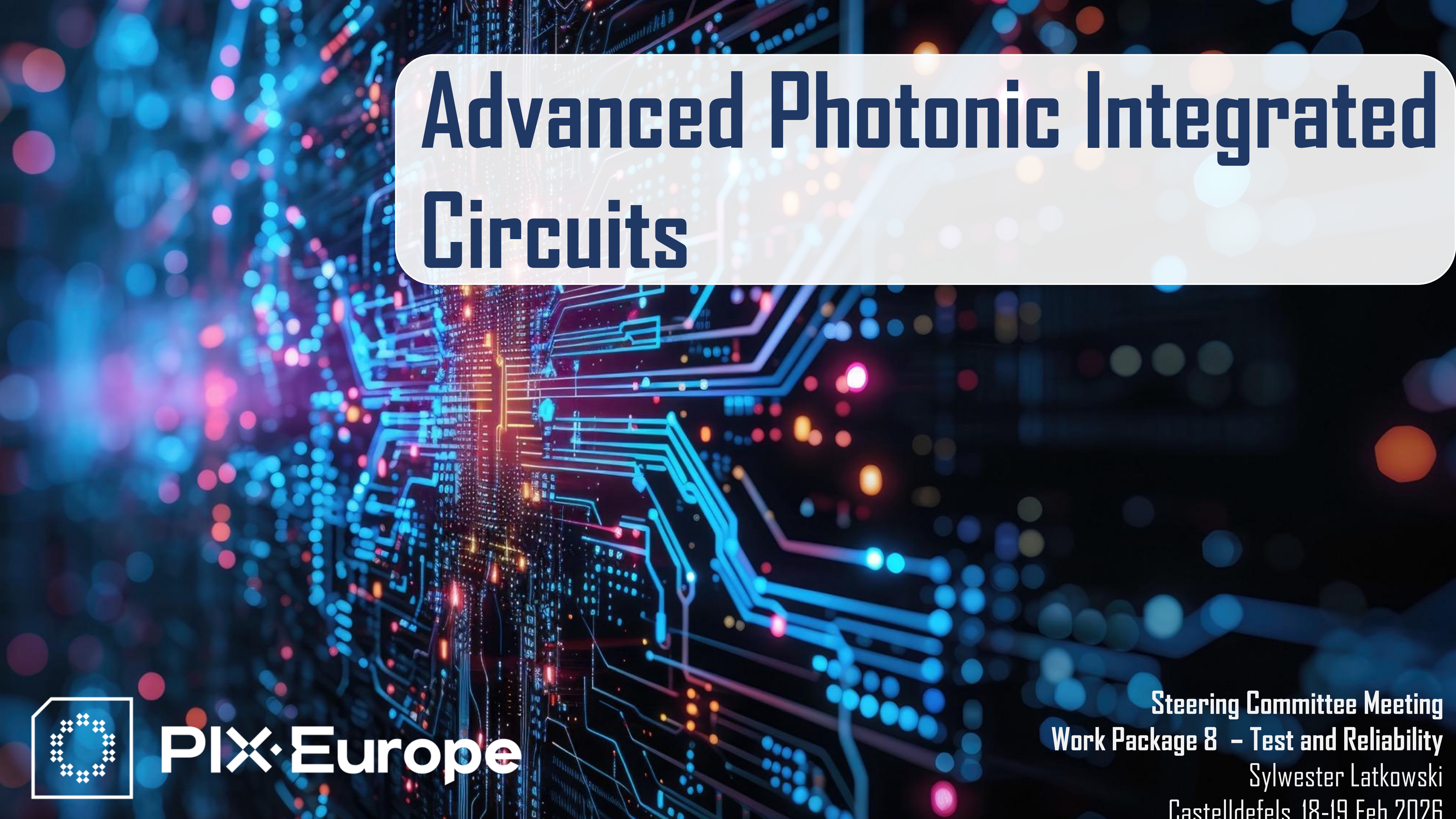


Advanced Photonic Integrated Circuits

PIX·Europe

Steering Committee Meeting
Work Package 8 – Test and Reliability
Sylwester Latkowski
Castelldefels 18-19 Feb 2026

Consortium in WP8

SPAIN
ICFO – **Coordinator**
UPV
IMB-CNM (CSIC)
IMDEA
UVigo

THE NETHERLANDS
TU/e
TNO
UTWENTE

BELGIUM
IMEC
UGENT

POLAND
WUT

UNITED KINGDOM
UCAM
USOTON

PORTUGAL
IT

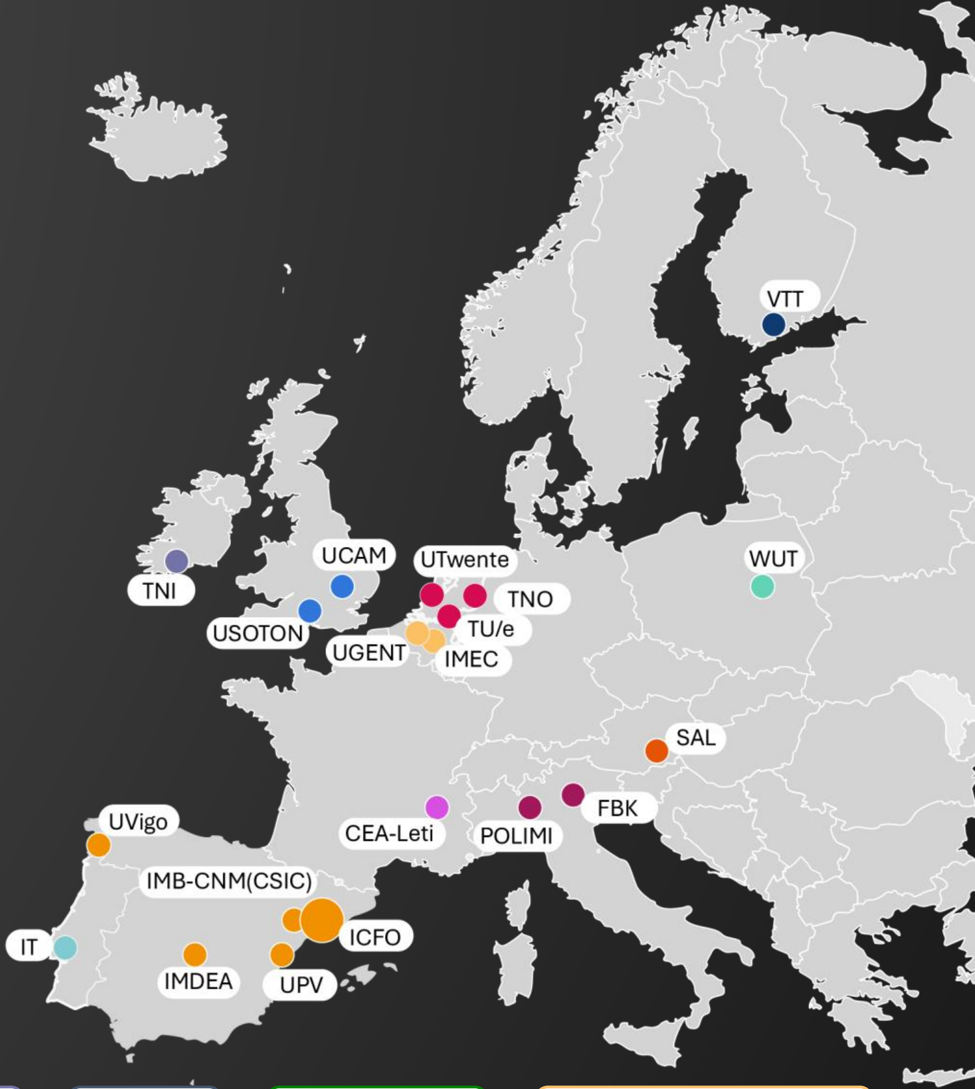
FRANCE
CEA-Leti

AUSTRIA
SAL

ITALY
POLIMI
FBK

FINLAND
VTT

IRELAND
TNI



Outline

1. Progress towards Objectives and Deliverable Status
2. Status of Work Package Activities
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Objectives summary (I)

- Measurement capabilities for materials and structure for determining layers, interface, structure, and morphology of PIC. Establish **functional test processes** at the building block level. Leverage the material characterization and test for the **identification of reliability issues** and analysis of **failure modes**.

- Establish capabilities for **in-production Wafer Level Test** at the Front-End and **Wafer Level Reliability** at the back-end-of-line (BEOL) at the pilot line level, supporting wafers **up to 300 mm** with the potential of scaling to **high volume manufacturing (HVM)**. Enable early in-production **failure modes identification**.

- Develop and optimize **test and reliability processes**, and methods for the Back-End. Establish test and reliability capabilities scalable from units to batches for **verification and validation** of assembly and packaging processes, from **subassemblies to modules**.

- Develop and implement new, direct, and indirect electronic-photonic characterization and test methods and solutions, supporting highly parallel electronic-photonics probing. Migrate advanced characterization methods into **rapid test processes** in the **front-end and back-end**, supporting **pilot and HVM production**.

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Objectives summary (II)

- Establish high throughput, **wafer-scale inspection** capabilities for in-production process validation and qualification for core and hybrid technologies. Utilize **machine-learning (ML)** methods to optimize process efficiency and maximize **throughput**.
- Develop solutions for rapid and accurate topography mapping and contactless probing for optical, RF, mmW, and terahertz signals. Employ **ML models** for **accelerated data classification** and analysis.
- Develop test and reliability methods for qualification of processes and PICs. Engage in **standardization** initiatives and technology **roadmaps** for **accelerated adoption** of integrated photonics by semiconductor microelectronics **supply chains** and application-specific **markets**.
- Develop, define, and implement **Test Design Kits** (TDK) following open standards, capturing the test and reliability process developed, and data obtained in this work package. Implement and demonstrate these in EDA environments, as **Design-for-Test** and **Design-for-Reliability** methodologies.

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WP8 Tasks

T8.1: Material and structure characterization

(**ICFO**, CSIC, TU/e, VTT, IMDEA, POLIMI, CEA-LETI, UCAM)

Set baseline processes on the tools and systems for material composition analysis, layers, and interfaces characterization, and for PIC structure and morphology characterization. Development and optimization of processes and recipes for studying the materials involved in the PIXEurope Pilot Line.

T8.2: Wafer Level Test and Reliability

(**UPV**, CSIC, TU/e, ICFO, TNI, VTT, CEA-LETI, IMEC, UVIGO, USOTON, IT)

Development of methods to assess the photonic performance is required, wafer-level, and amenable for inclusion in intermediate steps of PIC fabrication, dealing with the increasing complexity of monolithic PIC technologies and hybrid integration technologies combining several chip platforms.

T8.3: Package level test and reliability

(**TNI**, TU/e, ICFO, CSIC, UPV, VTT)

Establish and validate testing frameworks and reliability assessments for photonic packages with a focus on back-end processes for all the relevant photonic technologies to be developed in PIXEurope.

WP8 Tasks

T8.4: Test methods and protocols for High Volume Manufacturing (HVM)

(**UVIGO**, TU/e, CSIC, UPV, TNI, POLIMI, CEA-LETI)

Development of scalable methods, processes, and capabilities. Migrate advanced characterization methods into rapid test processes in the front-end and back-end, supporting pilot and HVM production flows.

T8.5: Contactless and visual inspection

(**IMDEA**, TU/e, UPV)

Development of technologies for high-resolution contactless inspection, and contactless optical and RF probing. Enabling rapid anomaly detection, defect-to-performance/reliability correlations at multiple process stages.

T8.6: Qualification methods and Standardization

(**TU/e**, TNI, CEA-LETI, UPV, USOTON, IT)

Reliability and test methods developed in PIXEurope will utilize open standards frameworks and will be streamlined into photonics and microelectronics industry roadmaps.

T8.7: Design for Test and Reliability

(**IT**, TU/e, UPV, ICFO, TNI, VTT, UVIGO, CEA-LETI, POLIMI)

Enable test and reliability implementation at the design stage in a product creation flow, through the definition of process Design Kits accounting for test and reliability, creating Test Design Kits (TDK).

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Tasks and partners involvements

Task 8.1:	Material and structure characterization (**ICFO**, CSIC, TU/e, VTT, IMDEA, POLIMI, CEA-LETI, UCAM)	**M1-M60**
Task 8.2:	Wafer-Level Test and Reliability (**UPV**, CSIC, TU/e, ICFO, TNI, VTT, CEA-LETI, IMEC, UVIGO, USOTON, IT)	**M1-M56**
Task 8.3:	Package level test and reliability (**TNI**, TU/e, ICFO, CSIC, UPV, VTT)	**M24-M56**
Task 8.4:	Test methods and protocols for HVM (**UVIGO**, TU/e, CSIC, UPV, TNI, POLIMI, CEA-LETI)	**M12 - M48**
Task 8.5:	Contactless probing and visual inspection (**IMDEA**, TU/e, UPV)	**M18-M56**
Task 8.6:	Qualification methods and Standardization (**TU/e**, TNI, CEA-LETI, UPV, USOTON, IT)	**M24-M60**
Task 8.7:	Design for Test and Reliability (**IT**, TU/e, UPV, ICFO, TNI, VTT, UVIGO, CEA-LETI, POLIMI)	**M18-M60**

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Deliverables

D8.1	Application notes materials	ICFO	M24
D8.2	PIC characterization procedures and methods	ICFO	M60
D8.3	Methods for Wafer-Level Test and Reliability	UPV	M36
D8.4	Demonstration of WLT and WRL processes	UPV	M56
D8.5	Package Level Test processes and methods	TNI	M48
D8.6	Package, assembly, and chip-level reliability processes	TNI	M56
D8.7	Scalable test methods and processes	UVIGO	M24
D8.8	Relevance for the high volume manufacturing (HVM)	UVIGO	M48
D8.9	PICs contactless probing and inspection technologies	IMDEA	M30
D8.10	Contactless probing and inspection process automation for WLT	IMDEA	M56
D8.11	Standardization of test processes	TU/e	M48
D8.12	Qualification methods	TU/e	M60
D8.13	Test Design Kits	TU/e	M30
D8.14	Design for Test	TU/e	M60
D8.15	Photonic to processing data correlation	CEA-LETI	M54

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Progress towards objectives – subjective summary

- Two tasks (T8.1 and T8.2) are active from M1
- Remaining tasks commencing later in the activity (M12, the next one)
- No deliverables or milestones until M24

- Bumpy beginning for some partners, but most, if not all, are active now
- All active partners already work towards the objectives

- Within and cross WP alignments on planned developments and capabilities
    - Synergizing developments towards complementary capabilities.
    - WPs on Design, Open Access, Training, and the technical ones

- Intense but careful preparations for the deployment of capabilities,
    - Large equipment procurement
    - In tight communication with WPs on procurement and installation
    - In-house planning for facilities at hosting sites

- On-site hands-on training and experience exchange (between partners).

- Highlights captured in the progress report 2025

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General status updates

Coordination

Monthly WP8 teleconferences have been running since July 2025.
All partners are engaged and actively aligned on individual ambitions towards common objectives
WP8 Deputy appointed: UCAM (more details soon)

Alignment Actions

Synergies and dependencies between the WP8 tasks and other WPs are being identified
WP lead does, and with the Deputy, will comprehensively coordinate broad coverage of TRL levels towards pilot-scale solutions.

Task level

Task leaders started to pick up responsibilities at the task level
Bilateral discussions with the WP lead

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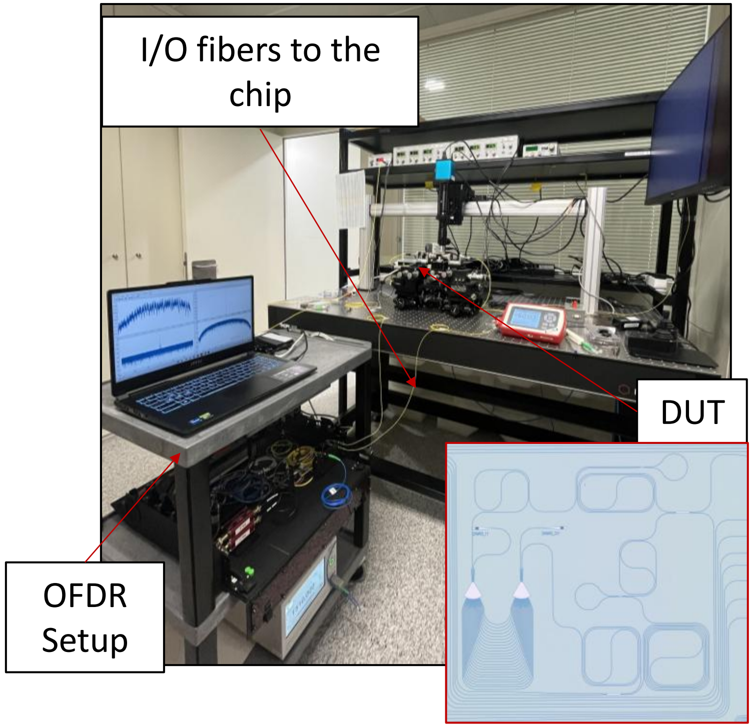
WP8 Universitat Politècnica de València - UPV

Main vision

- UPV will work **on in-fab wafer level testing (WLT)** using advanced **optical frequency domain interferometry (OFDI)** for the qualification of process parameters.

Activities

- **Automatic input/output optical coupling** tools and alignment routines.
- **Full-field measurements** (amplitude, phase, polarization) with ability to **identify events along chip/wafer paths**; **increased temporal/spatial resolution**
- Investigate new integrated structures to reinforce OFDI capacities
- **In-line** functional testing for monolithic and hybrid PIC technologies, via **grating couplers**, enabling inclusion at intermediate fabrication steps to monitor processes, detect issues early, reduce time and costs



Propietary OFDI/R setup @UPVfab facilities. Used to interrogate WLT test structures.

T8.2 Wafer-Level Test and Reliability (summary of on-going activities)

- **UPV – CNM collaboration:**
  - Implementation of wafer-level test (WLT) structures and OFDI-based measurement trials to strengthen testing capabilities.
- **Development of integrated test structures**
  - Multi-test architectures to enable automated wafer-level testing using OFDR / OFDI.
- **Test protocols and test tools under development**
  - To facilitate data management and analysis .
- **Ongoing procurement of key equipment**:
  - Tunable sources, optical spectrum analyzers, and alignment solutions for automatic and semi-automatic wafer-level-testing.

Planned contributions from IT: February 2026 update

- **WP4: design**
  - T4.5: Measurement-driven-model creation (UVIGO, IMEC, TU/e, IT, VTT, ICFO, CSIC, UC3M, POLIMI, FBK) M25-M60
  - T4.7: Access through Chips JU Design platform (TU/e, IMEC, IT, VTT, ICFO, UVIGO, CEA-LETI) M31-M60
- **WP8: Test & Reliability**
  - T8.2: Wafer-Level Test and Reliability (UPV, CSIC, TU/e, ICFO, TNI, VTT, CEA-LETI, IMEC, UVIGO, USOTON, IT) M1-M56
    - **IT** shall focus on developing test and measurement procedures based on OFDR to allow characterizing multiple devices from a single access point. In terms of hardware, such a goal shall involve designing low-loss and compact test points / access points into the PICs (together with the foundries) and developing matching 3D-printed optical probes. In terms of software, super-resolution methods shall be explored to enhance the resolution of OFDR measurements. In addition, better device characterization shall be sought by considering numerical modeling information as well as the designed layout on top of the OFDR traces. If possible, such techniques shall be used and demonstrated in the development of demonstrator 3 of WP9.
  - T8.6: Qualification methods and Standardization (TU/e, TNI, CEA-LETI, UPV, USOTON, IT) M24-60
  - T8.7: Design for Test and Reliability (IT, TU/e, UPV, ICFO, TNI, VTT, UVIGO, CEA-LETI, POLIMI) M18-M60
    - Besides aggregating all contributions of the participants of this task following PIXEurope's guidelines into developing PIXEurope's unified approach to Design Kit creation (see fig. 7), **IT** will develop novel test and measurement procedures starting from the development of a test design kit (TDK) with test-suitable packaging procedures, and culminating on OFDR characterization methods to allow characterizing multiple devices from a single access point.
- **WP9: Technology Validation & Demonstration**
  - **IT**: Participation in developing Demonstrator 3 (Next-Generation Small Form-Factor Pluggables for PON Optical Transceivers. **IT** shall participate in different parts of the development, namely system architecture, design of PIC and EICs, and testing.

- Work has begun, focusing on concept definition

- No updates
- IT will attend TUe's bootcamp on DKs
- *All partners will provide input to TDKs gathered from the developments of their contributions to tasks relevant tasks and work packages.*

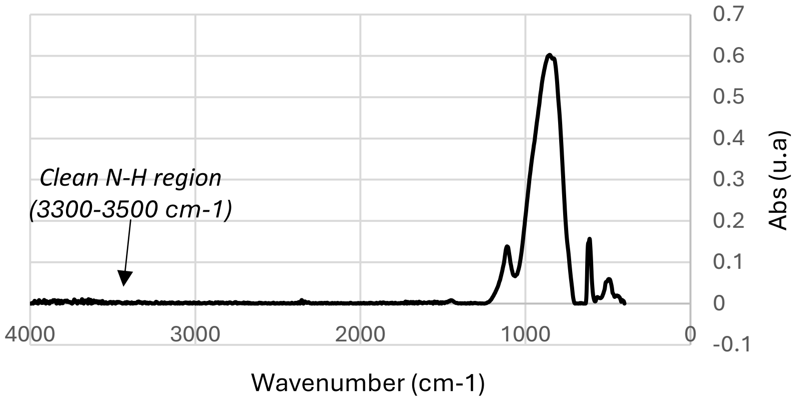
WP8 work in progress (CSIC)

Task 8.1 Material and structure characterization

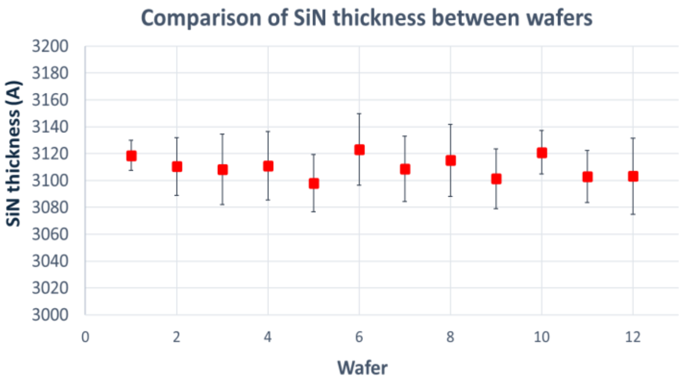
- SiN thin film characterization (thickness, stress, refractive index, FTIR) in the NIR and visible range, to be implemented in the design of passive components in WP5.
- aSi deposition and electro-optical characterization to be implemented in the design of modulators developed in WP5.

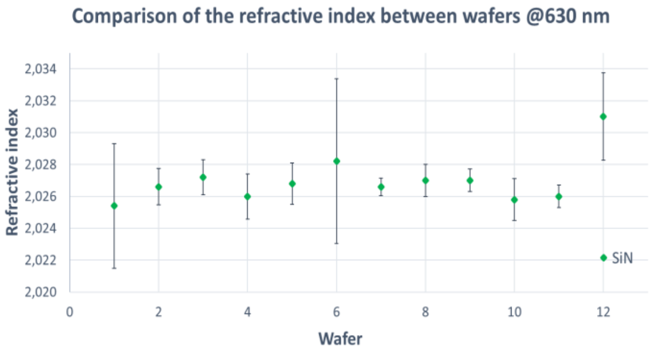
Task 8.2 Material and structure characterization

- Supporting UPV on the design and fabrication of structures for wafer-level characterization of photonic components.



FTIR spectra of SiOx (200nm) / SiN (300nm) stack





WP8 Test and Reliability: VTT's progress

Target review: In WP8, VTT is mainly planning to develop testing for its own 3 µm SOI PIC technology, which is targeted to support related services for PIXEurope's end users.

Progress:

- **Internal meeting procedures established**
  - Responsibilities divided into activities, each assigned to a person in charge
- **SiGe epitaxy**
  - Tender preparations for the new EPI reactor nearly ready (linked to WP3)
  - Simulations for SiGe composition initiated (linked to WP6)
  - Composition studies planned using methods such as SEM (EDX) or TOF-SIMS
- **Development of wafer-level testing**
  - Ongoing negotiations with tool vendors on upgrading existing probe station(s) to wafer-level optical coupling capability
  - Testing of 2PP-printed lenses for vertical coupling initiated

T8.3 Package Level Test and Reliability

- **Objectives (T8.3)**
  1. Develop qualification and lifetime testing methods for packaged and hybrid PIC assemblies.
  2. Establish package-level reliability protocols aligned with industrial practice.
  3. Provide reliability feedback to WP7 Packaging and support demonstrator validation (WP9).
- **Current Status**
  - Task formally starts in M24 – currently in preparation phase.
  - Aligning scope and equipment usage across WP7 and WP8.
  - Evaluating burn-in towers for packaged PIC lifetime testing and environmental chambers for thermal shock and temp/humidity testing.
- **Next 6 Months – Preparation Focus**
  - Define package-level reliability use-cases and draft preliminary stress profiles (temperature, humidity, ageing, vibration).
  - Specify requirements for burn-in towers/environmental test chambers.
  - Align reliability measurement metrics with TU/e (for future TDK integration) and identify first demonstrator candidates.

TNI 21 – Environmental test chambers
Thermal shock & temperature/humidity (climate) testing

TNI 20 – Burn-in tower
Reliability testing of packaged PICs

Updates from others
(even if brief do not underestimate the efforts)

- ICFO:
  - Tender published, next one to be published soon
  - ICFO Team at the experience exchange session at TU/e test development facilities
- UCAM:
  - Wafer-level characterization campaign with TU/e
- UVIGO
  - Equipment plans amendment
  - Bilateral planning optimization and site visit at TU/e planned
- CEA, USOTON, IDEMA in the report
- TUE:
  - Four tenders are being worked on, an internal tendering process is in place, fully aligned with procurement WP, technical specifications are drafted by experts, and vendors are approached for initial offers and negotiations
  - Expansion of laboratory facilities secured at HTC in full synchronization with the installation of TNO
  - Internal collaboration with the microelectronics reliability laboratory at TU/e established. Alignment with chip, module, and system-level reliability centers of expertise for optimum development and implementation in PIXEurope.
  - First hands-on experience exchange (training) delivered. Discussions with TNI on input to the training efforts.
  - Preliminary wafer-scale experiments with partners are agreed on and being scheduled,
  - Systematic poking, annoying, and helping partners, as well as engaging with other WPs - aka WP coordination

- More updates in the report prepared at the end of 2025, which can be found at :
  - ICFO SharePoint 05. Reports

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Challenges and mitigation

Key Challenges

1. The time – optimistic schedules vs reality of execution
2. Rolling engagement of the partners
3. From equipment procurement to established and validated capabilities
4. Broad TRL of ambitions within the WP8, but also other technical WPs
5. Open Access implementation of capabilities developed (an offered)

Mitigation

1. Constant alignment with other partners and WPs
2. Task leaders prompted to pick up and stimulate partners' engagement at a task level
3. Tight coordination with respective WPs (procurement, installation), support partners
4. WP lead, and Deputy will comprehensively cover TRLs and will monitor and correct implementation at the intra and inter WP levels.
5. Engage and clarify with respective WPs, Project coordinator (and MCT?)

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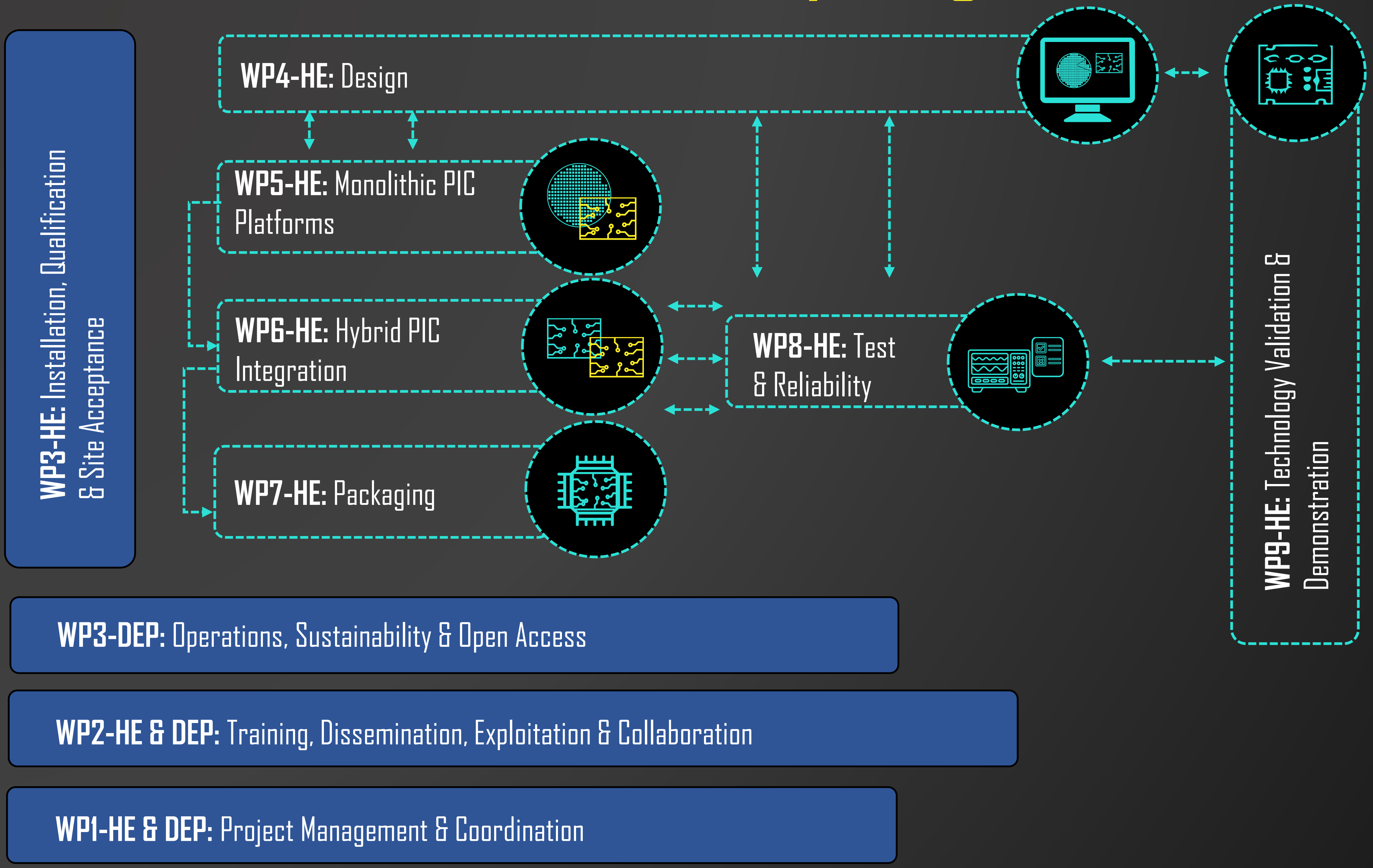
WP8 interaction with the rest of workpackages



WP3-HE: Installation, Qualification & Site Acceptance

WP4-HE: Design

WP5-HE: Monolithic PIC Platforms

WP6-HE: Hybrid PIC Integration

WP7-HE: Packaging

WP8-HE: Test & Reliability

WP9-HE: Technology Validation & Demonstration

WP3-DEP: Operations, Sustainability & Open Access

WP2-HE & DEP: Training, Dissemination, Exploitation & Collaboration

WP1-HE & DEP: Project Management & Coordination

The **Chips JU Pilot Line** is funded jointly by the **Chips JU**, through the European Union’s Digital Europe program and Horizon Europe program, as well as by the Participating States: Spain, Ireland, The Netherlands, Finland, Germany, Portugal, Poland, Austria, Italy, France, United Kingdom. In particular, this contract has received funding under Grant Agreement No. 101213727 and No. 101213744, and is co-funded by Spain through the Ministry for Digital Transformation and Civil Service under reference CJU-010000-2025-0005, as part of the Recovery, Transformation and Resilience Plan (PRTR).

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