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Photonic Packaging (WP7)

Peter O’Brien
Padraic Morrissey

September 16th, 2025

Agenda

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2. Description & Objectives
3. Deliverables
4. Packaging Inputs and Outputs
5. Partner Roles
6. Reference PICs & Packaging Examples
7. Discussion and Next Actions
8. Any Other Business

Attendance and Introductions

- **TNI (WP Lead):**
  - Padraic, Liz, How Yuan, Peter
- **ICFO (Deputy):**
  - Armand, Giovan
- **TU/e:**
  - Sylwester
- **VTT:**
  - Timo
- **UVIGO:**
  - Roi
- **IMEC:**
  - Peter
- **CSIC:**
  - Carlos, Pau
- **UC3M (IMDEA networks):**

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Description & Objectives

1. Develop **advanced package-level** and **wafer-level processes** to overcome bottlenecks in PIC manufacturing.
2. Create **multiphysics simulation and design models** (optical, electrical, thermal) validated with prototypes.
3. Prepare materials, specialised tooling, and bonding/connector processes (**non-epoxy**, pluggable, 3D-printed, **advanced polymers/ceramics**).
4. Introduce **wafer-level co-packaging** with **electro-optical interposers** and high-precision **die-to-wafer flip-chip** assembly.
5. Fabricate **reference PICs and EICs** to validate processes and deliver packaged demonstrators.
6. Collect **packaging design rules** and formalise into **Assembly Design Kits (ADKs)** for integration with design and test flows.

Tasks

- **T7.1 Package Simulation & Design** (**UC3M**, TNI, ICFO, TU/e, M1–M54)
  - Holistic multiphysics models (optical, electrical, thermo-mechanical), validated with prototypes.
- **T7.2 Package-Level Processes** (**TNI**, ICFO, UVIGO, UC3M, M1–M50)
  - Non-epoxy bonding, pluggable optical connectors with microlens arrays, 3D-printed polymer packages.
- **T7.3 Wafer-Level Processes** (**TNI**, ICFO, UC3M, IMEC, M6–M60)
  - Electro-optical interposer co-packaging, transfer printing, high-precision flip-chip (±1 µm), 2D pluggable optical connectors.
- **T7.4 Electro-Optical Interposers & Reference Chips** (**TNI**, ICFO, UC3M, VTT, TU/e, M6–M54)
  - Interposer development (glass/polymer, micro-optics integration), and fabrication of Si, SiN, InP reference PICs and EICs.
- **T7.5 Packaging Materials** (**UVIGO**, TNI, ICFO, M1–M48)
  - Preparation of bonding/printing equipment, polymers (LCP, PEEK), ceramics (AlN, Al_2O_3), pluggable connectors, validation with reference chips.
- **T7.6 Packaging Design Rules & ADKs** (**TU/e**, TNI, ICFO, UC3M, UVIGO, M18–M60)
  - Collect rules from tasks, formalise into ADKs for package- and wafer-level processes, link to WP8.

Packaging: Inputs and Outputs

Work Package	Inputs to WP7	Outputs from WP7
WP4 – Design	PDKs incorporating packaging constraints	ADKs with packaging design rules, compatible with design flows
WP5 – Monolithic PIC Platforms	Technology (Si, SiN, InP, etc.) Open Q: where are PICs fabricated WP5 or WP7	Feedback on alignment, bonding, pad layouts for packaging optimisation
WP6 – Hybrid PIC Integration	Hybrid PICs with novel materials and structures	Packaging processes adapted to heterogeneous chips
WP8 – Test & Reliability	Test requirements, reliability protocols	Packaged devices for evaluation; packaging rules feeding into TDKs
WP9 – Demonstrators	Demonstrator specifications (performance, interfaces)	Fully packaged PIC/EIC modules for demonstrator systems
WP3 – Operations & Open Access	Framework for open access service delivery	Standardised packaging processes and ADKs integrated into MPW services
WP3 – Training & Dissemination	Training structures, dissemination channels	Packaging methods and demonstrator examples for training and outreach

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Partner Roles (summary)

- **TNI (Lead):** Overall responsibility; package/wafer-level processes; EIC reference chips; demonstrators; transfer to manufacturing.
- **ICFO:** Design & development of electro-optical interposers, micro-optics; prototype validation.
- **UC3M:** Multiphysics models, simulation optimisation, high-density RF interconnect design.
- **TU/e:** Collect design rules, formalise into ADKs, ensure simulation–design flow compatibility.
- **VTT:** Development of PIC reference chips (Si, SiN, InP).
- **UVIGO:** Novel packages via 3D printing and advanced materials (LCP, PEEK, ceramics).
- **IMEC:** High-precision die-to-wafer flip-chip processes in iSiPP300 platform.
- **CSIC:** Provision of SiN reference PICs, aligned with WP7 technical requirements.

Partner Roles – Tyndall

- **Intro**
  - Tyndall National Institute is Ireland's leading research centre for photonics and advanced electronics. Within PIXEurope, Tyndall leads WP7 and brings expertise in optical packaging, wafer-level integration, and advanced process development.
- **Main objectives (T7.2, T7.3, T7.4)**
  - Develop and optimise package-level processes (non-epoxy bonding, pluggable connectors).
  - Lead development of wafer-level packaging flows (electro-optical interposers, flip-chip assembly, 2D pluggable connectors).
  - Work with ICFO in T7.4 on development of glass interposers and validation of coupling schemes.
- **Actions in Q4 2025**
  1. Begin preparation for non-epoxy bonding and pluggable connector concepts.
  2. Scope the wafer-level packaging flow, including interposer and flip-chip processes.
  3. Provide initial update on equipment status and readiness at Tyndall.
  4. Coordinate with ICFO on interposer material options (glass/polymer) and early modelling needs.

Partner Roles – ICFO

Organization: ICFO, Institute for photonic sciences, based in Barcelona (Spain). Project Coordinator.
ICFO hosts 25 research groups, with more than 400 researchers. Research at ICFO range from fundamental to applied optics, with great focus on quantum communication, medical optics, photovoltaics and nanomaterials.

Objectives in WP7:

- Design and development of the electro-optical interposer (especially optical waveguides and electrical routing)
- Glass micro-machining for micro-optics compatibility (align with TNI)
- Simulation and modelling of packaging
- Prototyping of packaged devices and interposers for modelling validation

Actions in Q4 2025:

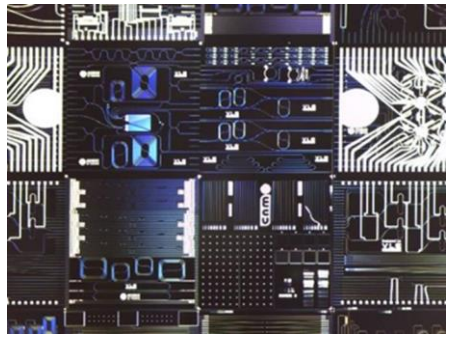
- Alignment with partners about interposer optical structure (cross section, waveguide type, coupling, micro-optics)
- First modelling of interposer optical waveguides
- Definition of packaging models to be developed

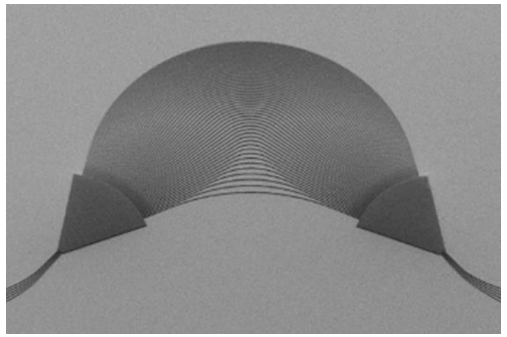
Partner Roles – CSIC

- **CSIC** brings its technological expertise in silicon nitride PICs for NIR and Visible from the IMB-CNM photonics platform. SiN PICs developed in WP5 and WP6 will be brought forward to WP7, in accordance to WP7 tasks specifications and needs.

- **CSIC**'s objective in WP7 is to provide SiN reference PICs, in accordance to WP7 stakeholder technical requirements and timelines.

- **Expected actions during Q4 2025**: alignment with WP7 partners regarding SiN PICs.
  - Identify direct collaborators in WP7
  - Define SiN PICs requirements for WP7
  - WP7 task planning regarding SiN PICs





Centro Nacional de Microelectrónica IMB

CSIC
Consejo Superior de Investigaciones Científicas

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Conventional and Disruptive Packaging

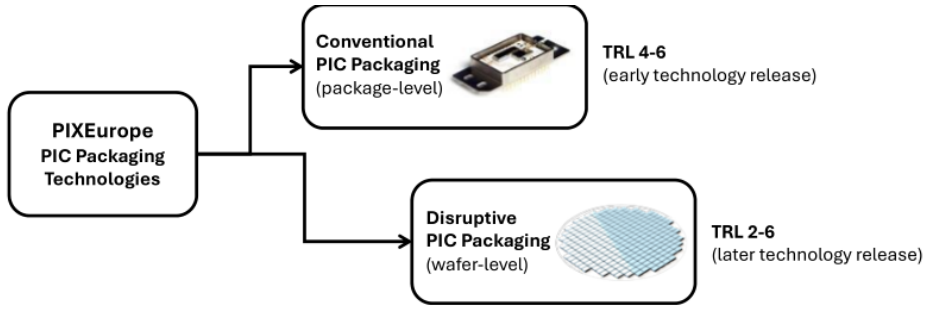


***Figure 6**: PIXEurope will address the PIC packaging bottleneck by following two complementary approaches. First, we will enhance the reliability and manufacturing of conventional (package-level) packaging technologies. Second, we will develop breakthrough wafer-level packaging technologies suited for ultra-high levels of integration and mass production. The combination of both these approaches will enable us to release in-demand technologies early in the project, followed by more advanced and highly scalable technologies towards the end of the project.*

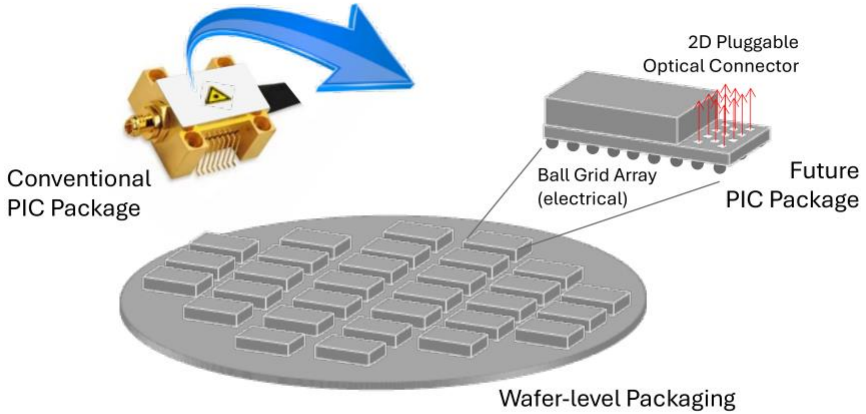
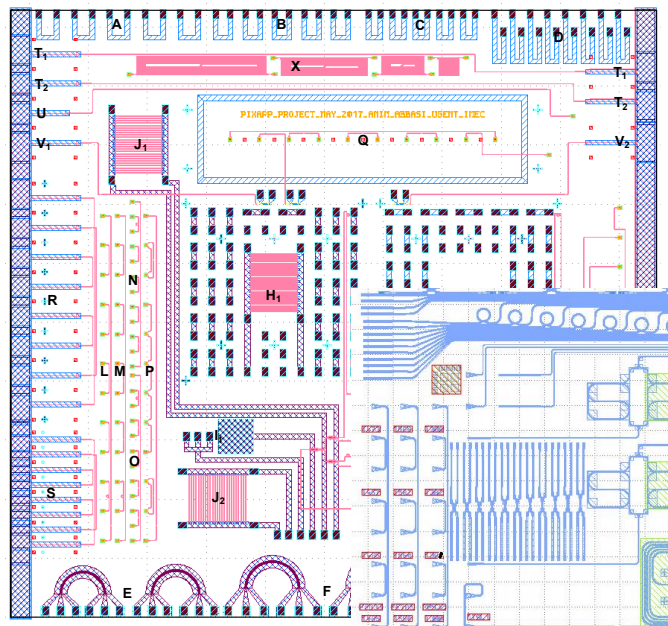


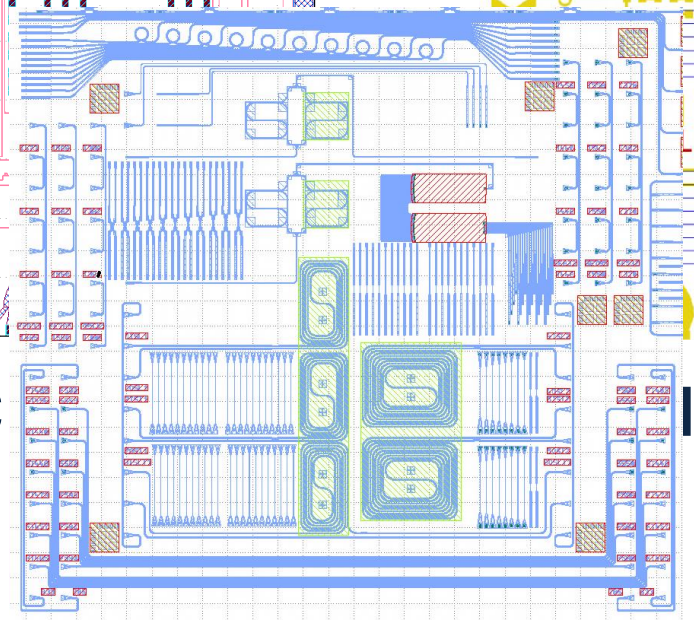
***Figure 44**: Wafer-Level packaging of PIC and electronic chips on an electro-optical interposer and sealing to form a hermetic package. The interposer is electrically connected via solder bumps (ball grid array format) and optically connected via a 2D array surface pluggable connector. A conventional butterfly-style package is shown for comparison.*

Package Parameter	Package-Level PIC Packaging	Enhanced Package-Level PIC Packaging	Disruptive Wafer-Level PIC Packaging
Optical Packaging	Bonded fibre arrays 1-3 dB coupling loss < 100 connections	Bonded & pluggable fibre arrays Microlens arrays for free space applications < 1dB coupling loss < 100 connections	Pluggable 2D fibre arrays Microlens arrays for free space applications Optical connections with electro-optical interposer < 1dB coupling loss >> 100 connections
Electrical Packaging	< 100 connections (typical max)	< 100 connections (typical max)	Electrical connections with electro-optical interposer >> 100 connections
Package Process & Cycle-time	Package-level process with typical assembly time of 10 mins per package	Package-level process with typical assembly time of 5 mins per package	Wafer-Level process with typical assembly time < 1 min per package
Package Reliability	Epoxy used for optical packaging major reliability issue	Epoxy-free optical packaging increases reliability based on solder bonding process	Epoxy-free optical packaging based on wafer-level bonding process
Package Application & Volume Requirements	Speciality markets (e.g. space, medical) typically 100-1000s of units per run	Speciality markets (e.g. space, medical) typically 100-1000s of units per run	Mass markets (e.g. AI, AR/VR, data centres, consumer, handheld devices) >> 1000s of units per run Ideal for co-packaging requirements
Package Mechanical Design	Expensive (e.g. butterfly-style package), especially for prototyping	Less expensive (LCP polymer), ideal for fast prototyping and transition to manufacture	Wafer-Level BGA-style suited to multi-project runs for shared users and scaling to mass volumes
Package Design Rules & Predictive Models	Limited design rules with basic package models	More advanced design rules with ADKs and highly developed multi-physics package models	More advanced design rules with ADKs and highly developed multi-physics package models

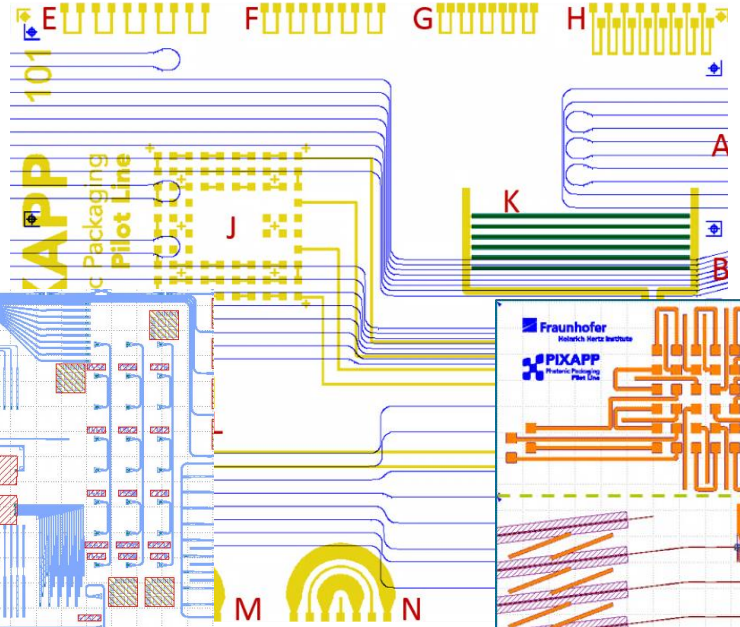
Reference PICs & Packaging Examples



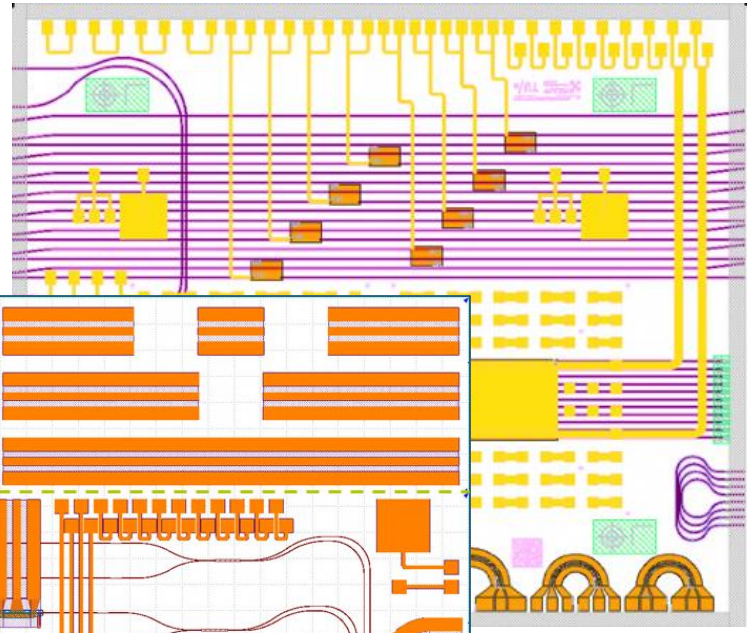
SOI-PIC



SiN-PIC (IMEC)



I-PIC (Lio



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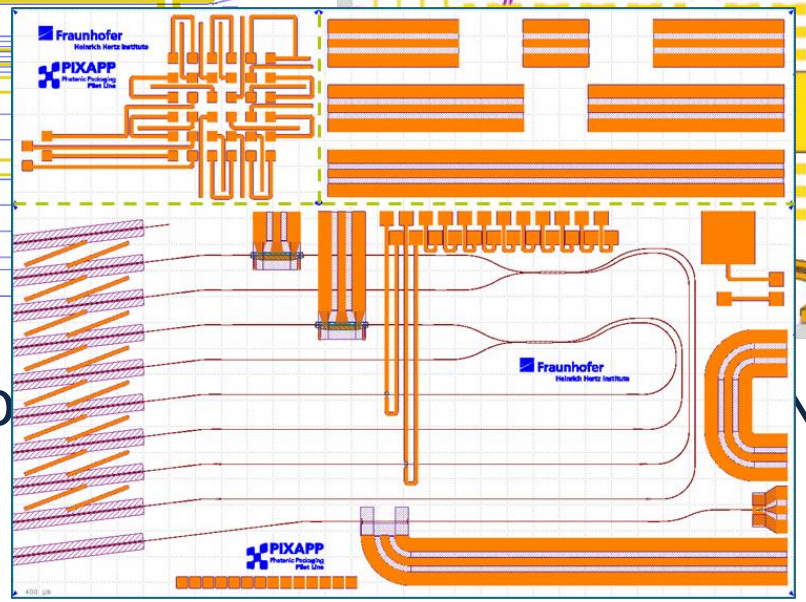

InP-PIC (HHI)

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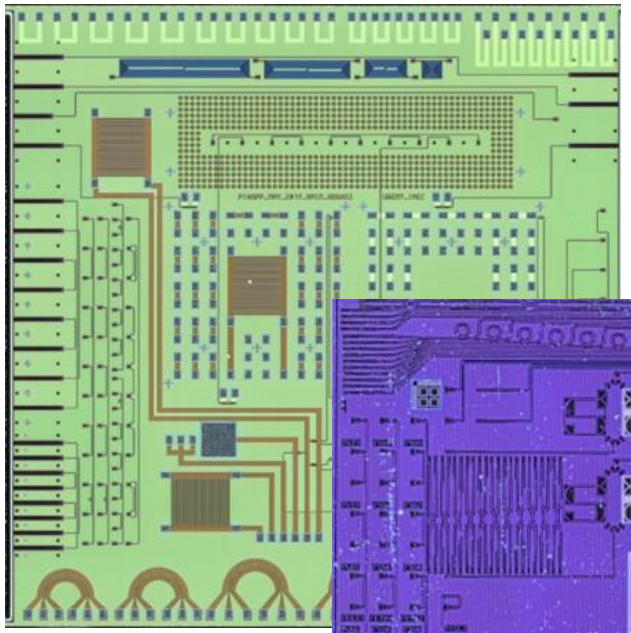
Reference PICs & Packaging Examples



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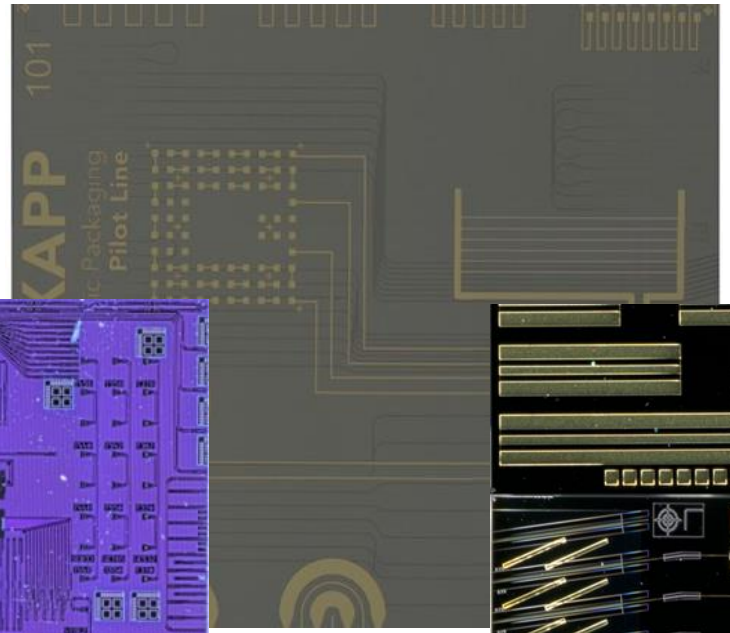

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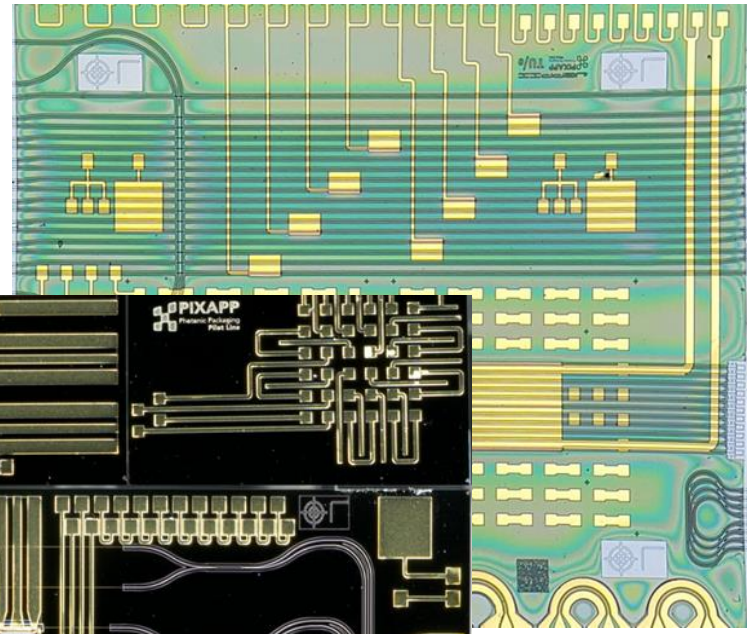

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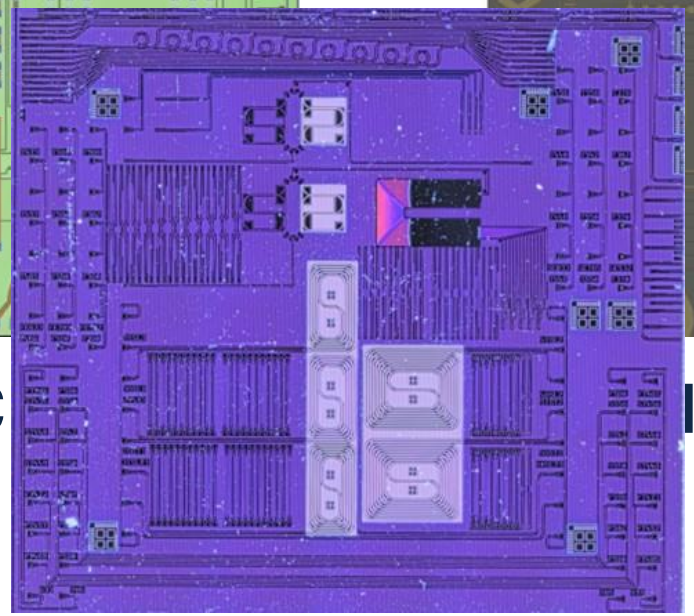
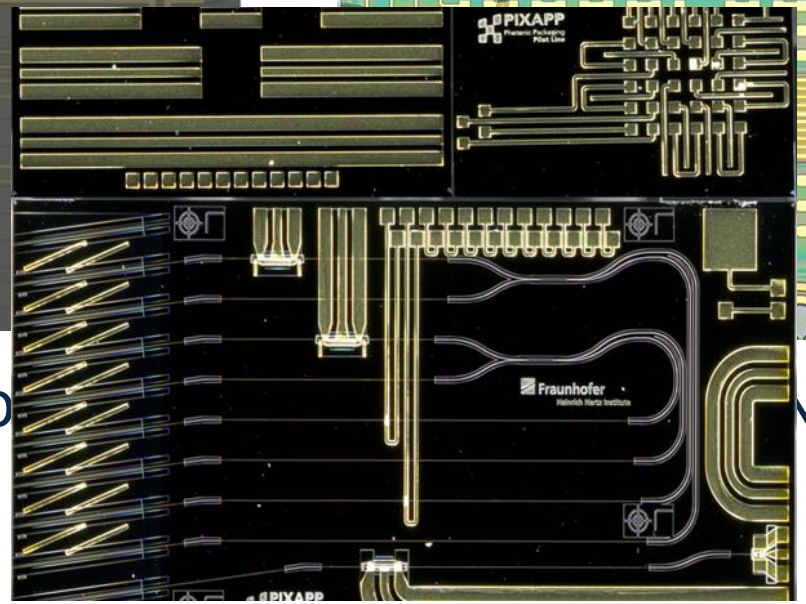


SiN-PIC (IMEC)



InP-PIC (HHI)

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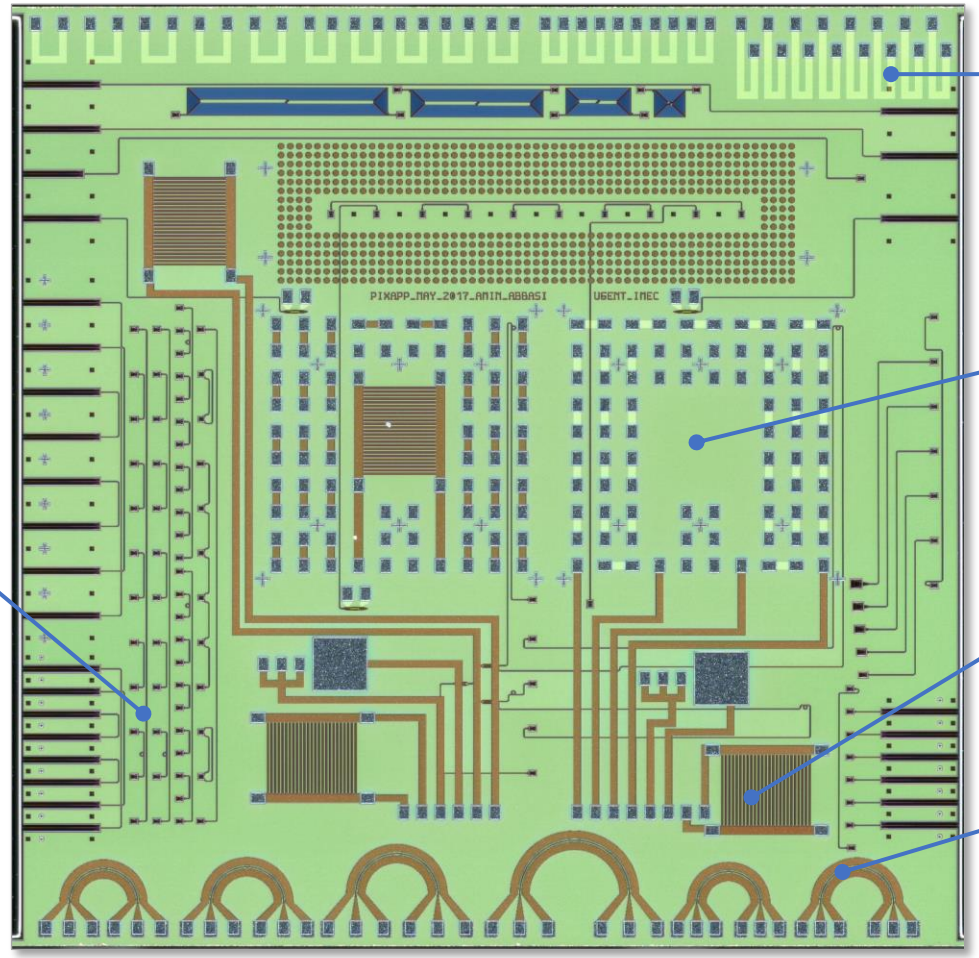
Reference PICs & Packaging Examples



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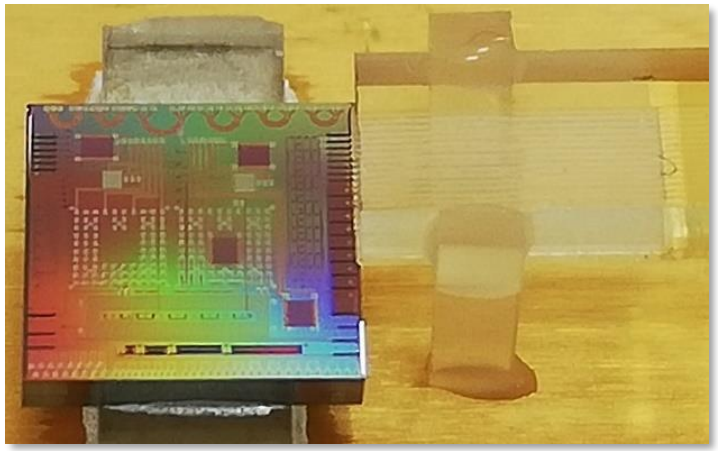
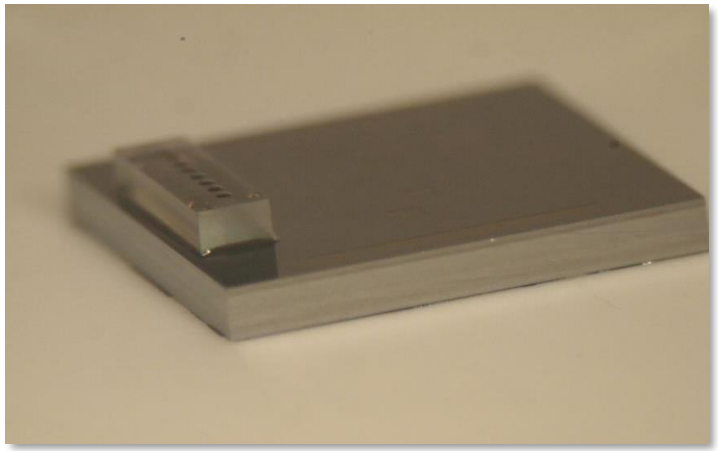
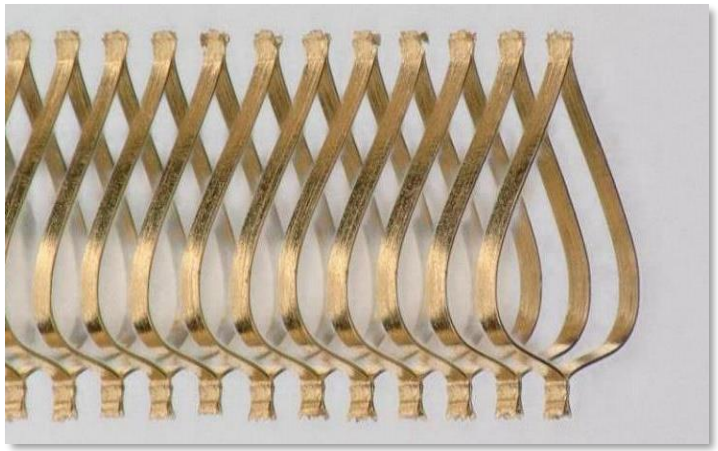
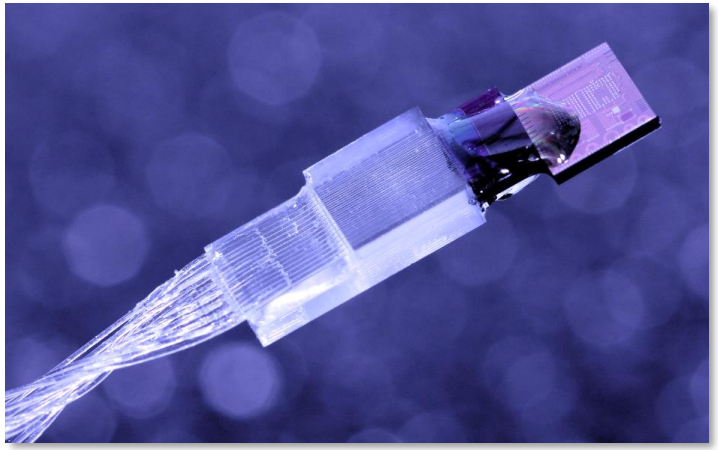
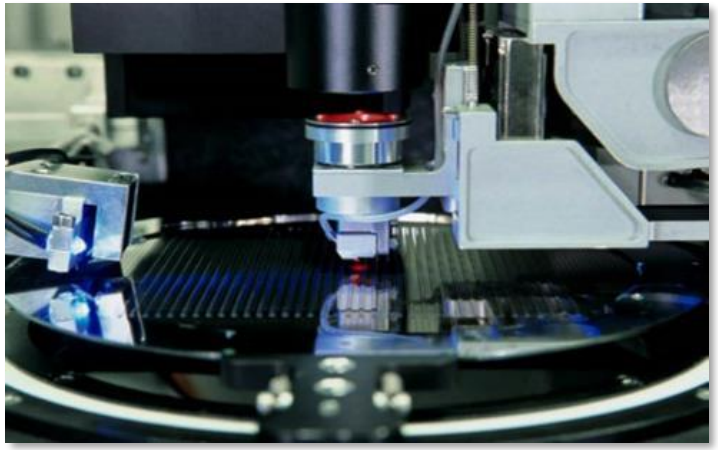
Reference PICs & Packaging Examples

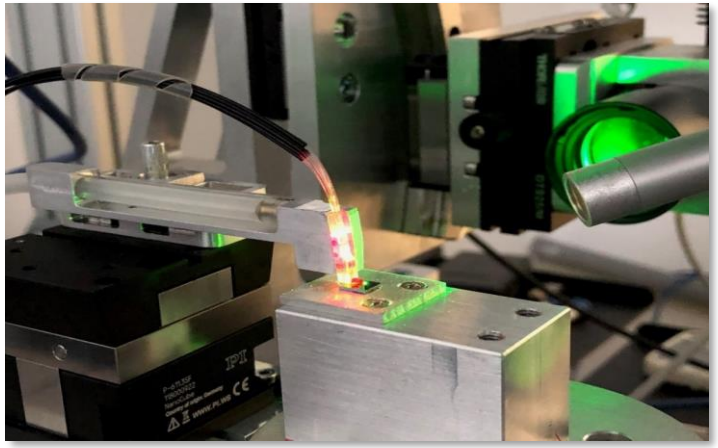












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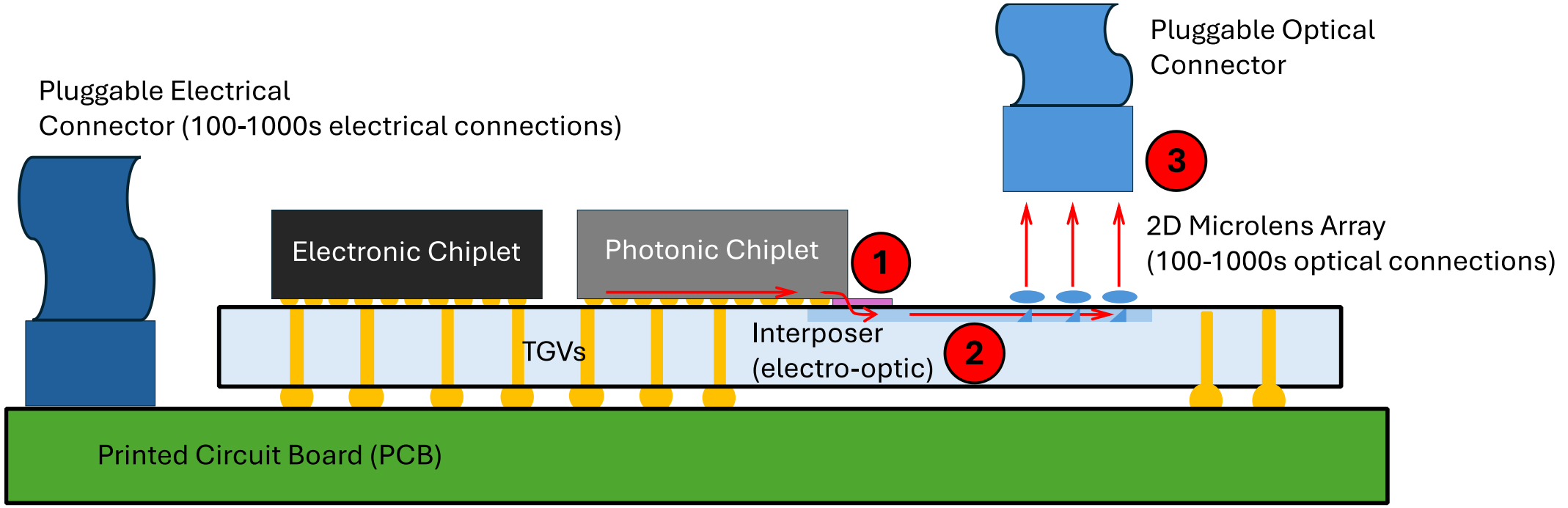
Wafer Level Packaging



PIXEurope will develop **three core packaging technologies** to enable wafer-level co-packaged photonic-electronic modules with 100-1000s of optical and electrical connections. This includes 1) **PIC chips designed for surface-level optical coupling**, 2) **flipchip packaging on electro-optical interposers** with fan-out optical ReDistribution Layers (RDL), and 3) **2D arrays of microlenses enabling expanded beam pluggable connectors**.

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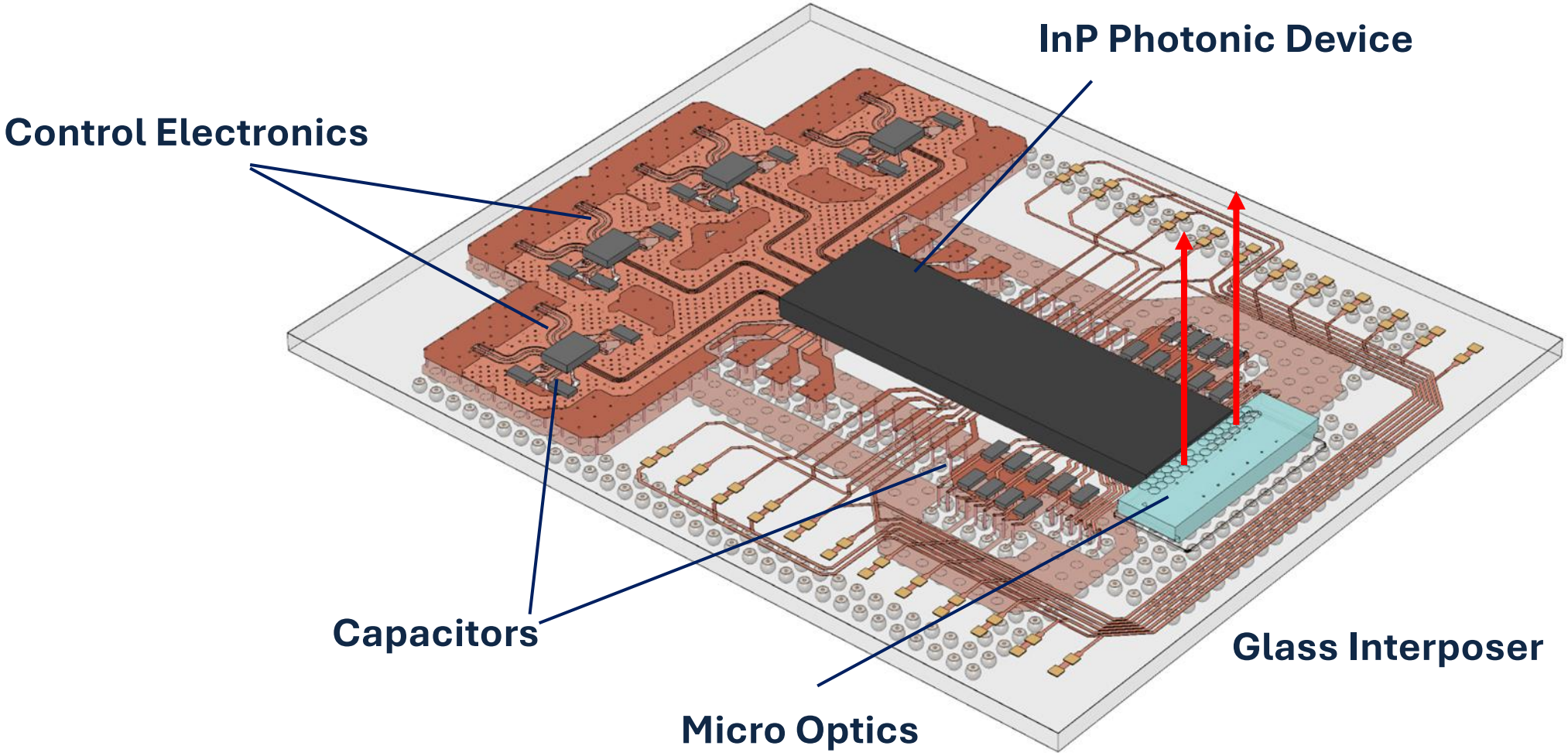
Wafer Level Packaging



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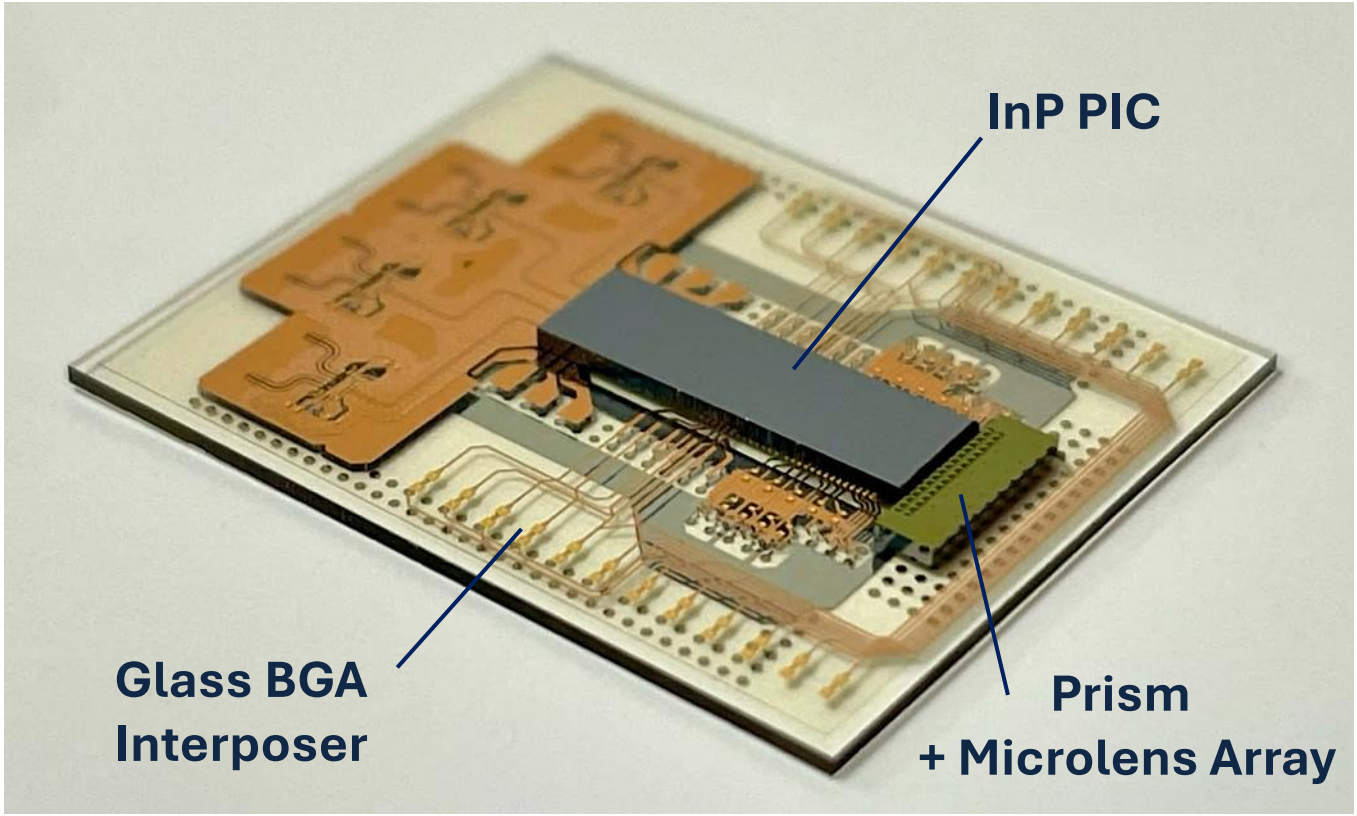
Wafer Level Packaging



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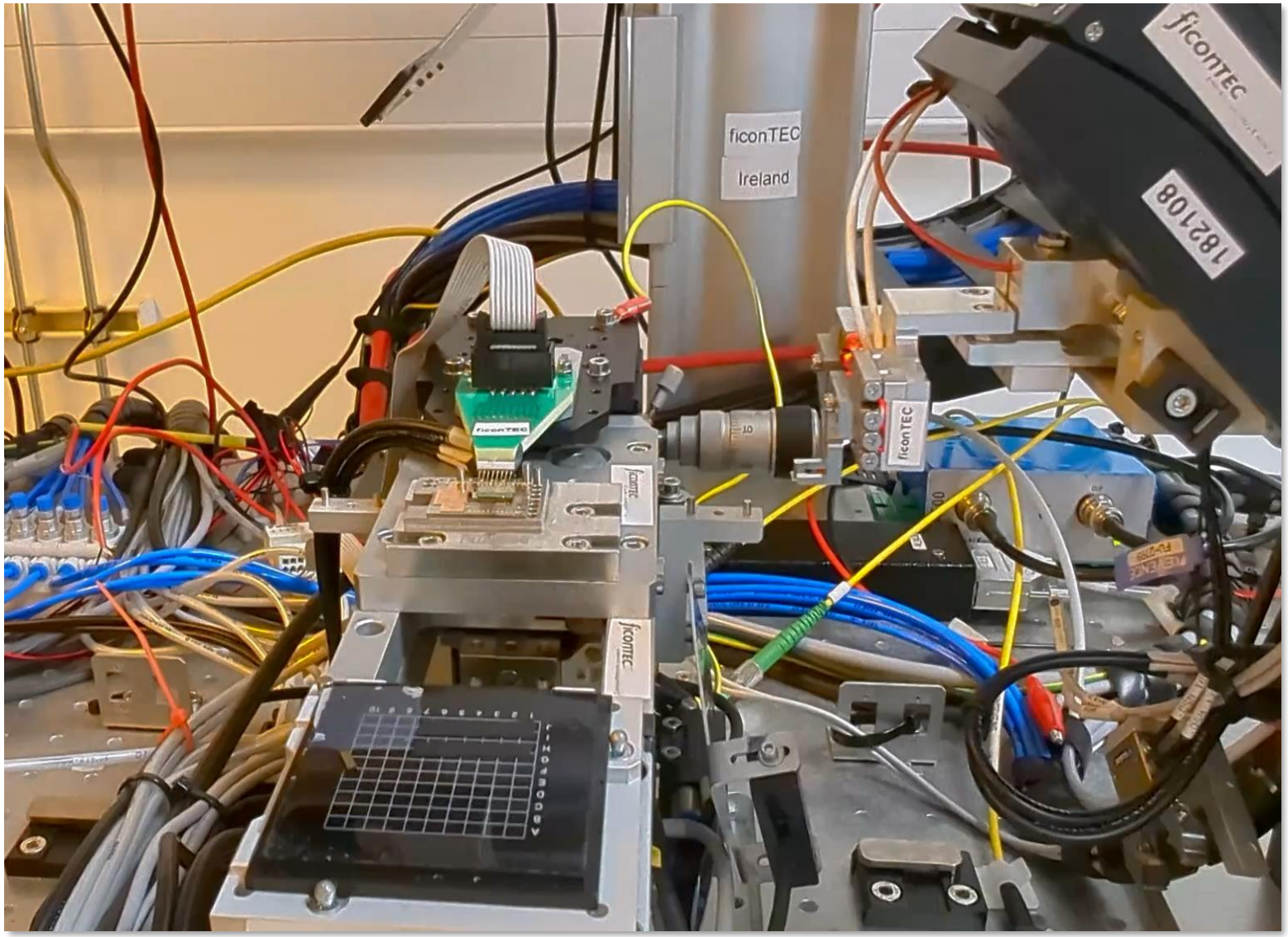
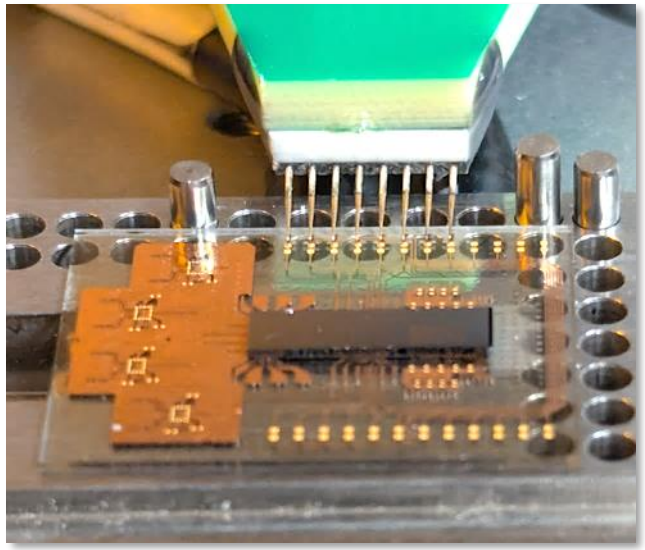
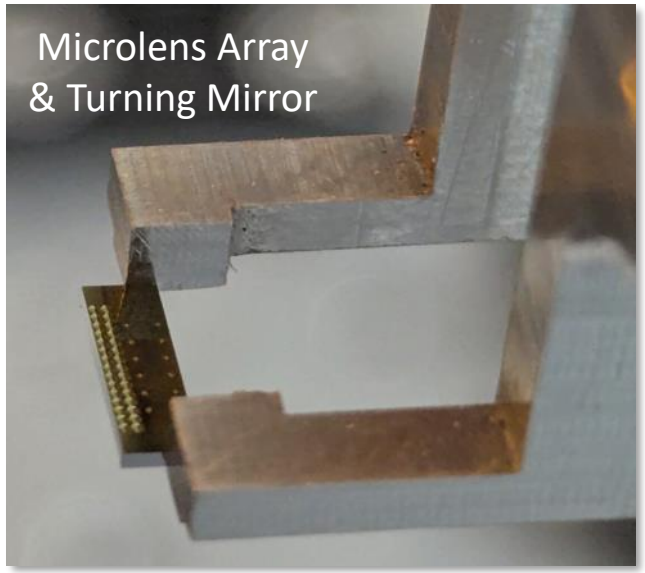
Wafer Level Packaging







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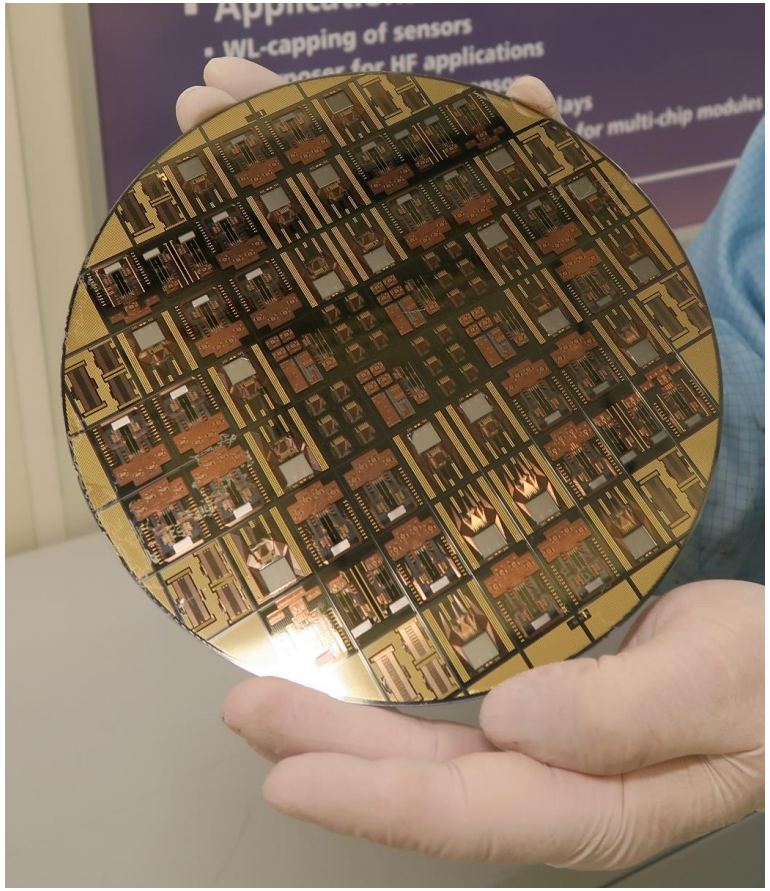
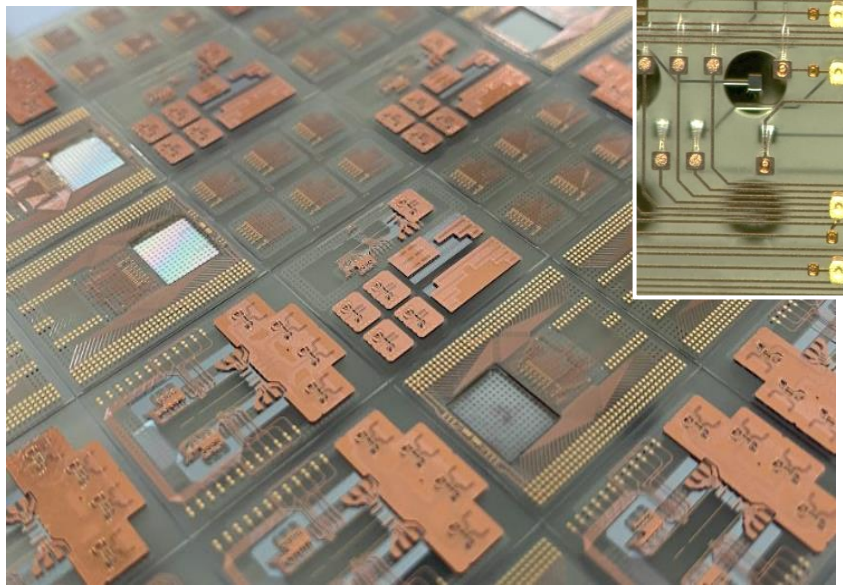
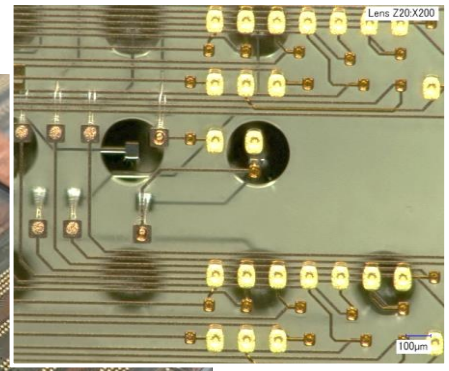
Wafer Level Packaging

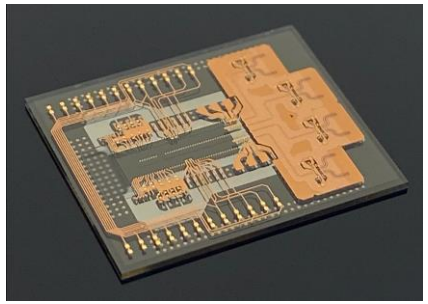


200mm Demo Glass Wafer Run Completed

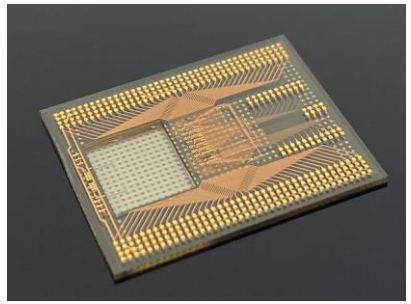




Interposer for InP PIC demo package



Interposer for Si PIC demo package



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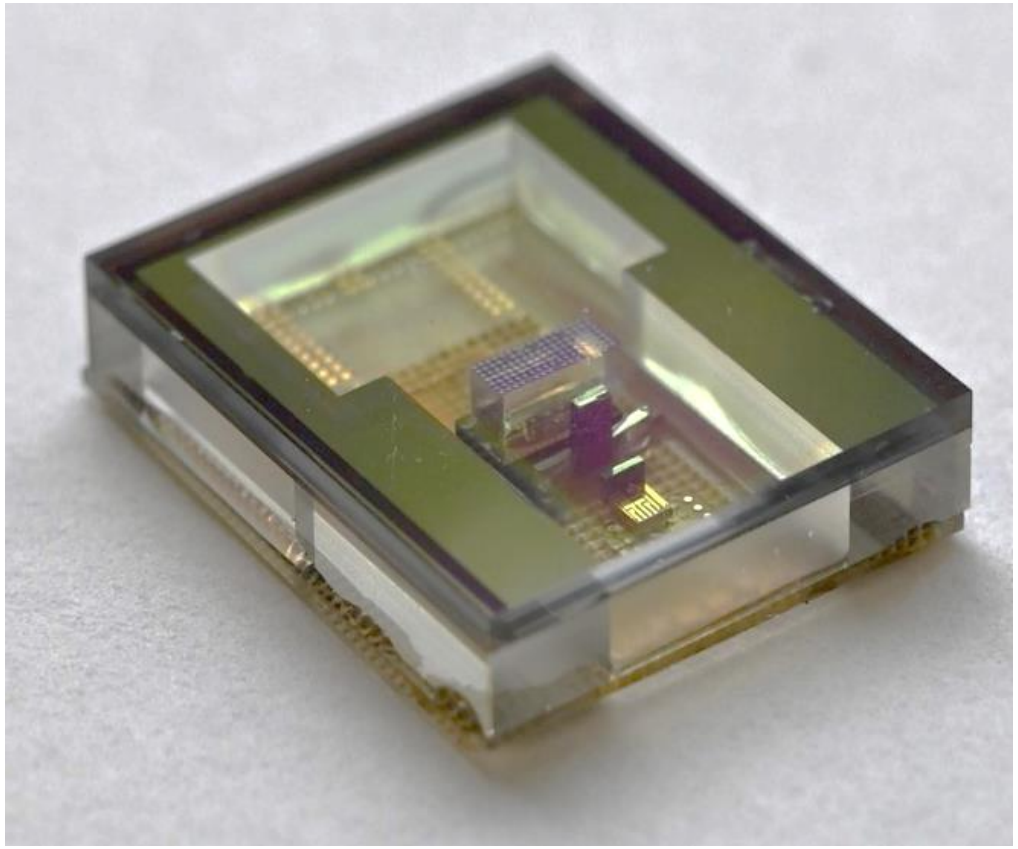
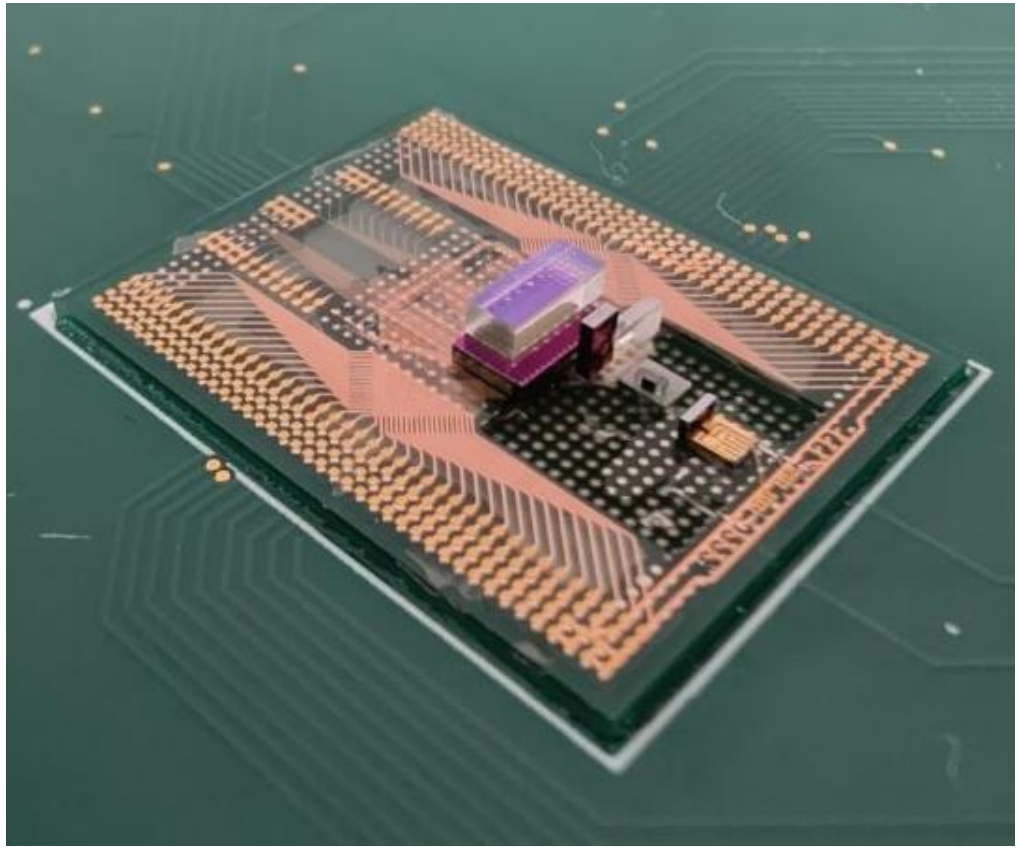
Wafer Level Packaging



Stand-alone package for Si PIC for electrical pluggable integration



Electronic board integrated package for Si PIC for end-user application

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Discussion and Next Actions

Discussion

- Any immediate concerns or questions from partners.
- Expectations for monthly WP7 meetings (format, focus, and level of detail).
- Early coordination needs with other WPs.

Before the Next Meeting (October)

1. WP7 task leads/co-leads: prepare short task outlines (aligned with proposal):
   - Objectives & scope
   - Initial plans & dependencies
   - Key actions for next 3–6 months
2. Tyndall: circulate Excel file to identify people per task; partners to complete
3. Partners: share initial notes on equipment status & timelines
4. Meeting: UVIGO + WP7 lead to define equipment and 3D printing requirements

Q4 2025 Actions

1. Begin early technical work where possible (simulation setup, concept development).
2. Continue discussions on reference PICs and EICs to clarify future requirements.
3. Share updates on equipment installation progress and readiness for packaging tasks.
4. Identify and map key interdependencies with other WPs (Design, Test, Hybrid).
5. Plan for early 2026 activities to support the next phase of packaging development.

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