# Advanced Photonic Integrated Circuits

**WP6 Monthly 01**

Online, 18 September 2025

PIX·EUROPE

# WP6 Kick-Off Meeting

## WP 6:
## Hybrid PIC Integration

## WP Leader & Deputy
Universitat Politècnica de València
Universiteit Gent

## Agenda

1. Welcome & intro (10 min)
2. Task presentation (3 min / task) (30-35 min)
3. How to: monthly meeting, activity report (10 min)
4. AoB (10-5 min)

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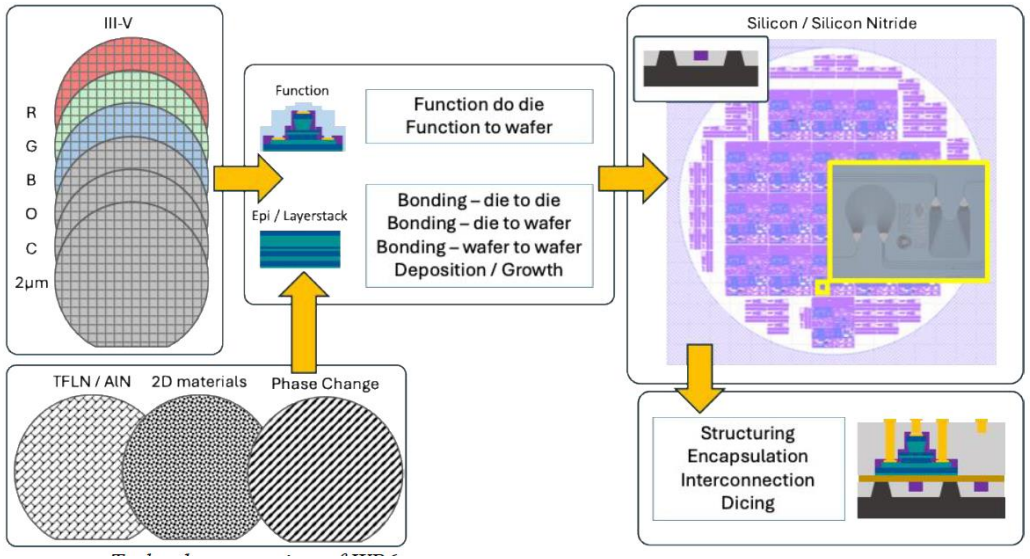
# 1. Intro / Aim & Objectives

**Aim:** To provide platforms with functions beyond the individual monolithic ones




**Objectives:**

1. Modular hybrid III-V on SiN, using MTP / LIFT
2. MTP of GaN and III-V coupons on SiN, for RGB
3. MTP of III-V, BIG, TFLN, BTO on thin Si
4. MTP of III-V and TFLN on thick Si
5. 2D LMs, CQDs, UTFMs and PCMS on Si, SiN, and Ge-on-Si
6. Structuring, litho, etching and dicing of hybrid PIC substrates

# 1. Intro / Objectives – Activity areas

| | |
|---|---|
| **Hybrid Integration** | Modular multi-band III-V MTP on SiN, including SOA |
| | O-band III-V die MTP on SiN |
| | Laser induced forward transfer (LIFT) III-V on Si |
| | MTP of active and passive functions onto Si photonics |
| **Novel Materials, Functions and Processes** | Colloidal quantum dots (CQDs) |
| | Thin-film lithium niobate (TFLN) |
| | Barium Titanate (BTO) |
| | Bismuth Iron Garnet (BIG) |
| | 2D layered materials (2D LM), including graphene |
| | Phase-change materials (PCMs) |
| | Ultra-thin metal films (UTMFs) |
| | Die copper pillars process modules |
| | Plasma dicing process modules |
| | Spot-size converter (SSC), Photodetector (PD) and Control Loop |

# Instructions sent (for completeness)

- Task name, start / end months, leader, participants
- Main global objective & brief description
- 3 bullet points of action / objective for 2025Q4

# T6.1 Multi-band O/C/2 µm III-V onto SiN (UPV, CSIC, TU/e) M6-M60

Main global objective: development of a hybrid III-V/SiN platform with different gain bands co-existing in a single chip.

Brief description:

- Material interface specifications: UPV and TU/e will jointly define the interface specifications between the CSIC SiN platform and TU/e-designed III-V SOAs. Vertical evanescent coupling will be co-designed considering lithography, etching, and transfer, with numerical simulations using tools like GDSfactory and tidy3D.
- Device design, patterning and transfer: TU/e will design III-V devices (epitaxy, metallization, patterning, coupon release), while UPV will work on SiN platform transfer. CSIC will provide 100 mm SiN wafers, and UPV will create dummy silicon technologies to validate designs before applying them to functional III-V coupons.
- Technology transition to 150 mm wafers: UPV and CSIC will transition part of the technology to 150 mm wafers. Hybrid multi-band PICs will integrate UPV's patented Si-pillar technology for thermal management, processed before SiN deposition. TU/e will receive ultra-flat SiN wafers with passive components for further InP+SiN hybrid integration experiments.

3 bullet points of action / objective for 2025Q4:

- Task kick-off to be appointed by UPV with TU/e and CSIC
- Identification of partner personnel involved with roles
- Outline of plan for 2026

# T6.2: III-V O-band die onto SiN (UPV, CSIC) M18-M60

Main global objective: development of III-V die transfer of un-patterned epitaxies onto SiN platforms.

Brief description:

- O-band epitaxy: will be specific for this task, and we will consider different methods of optical coupling (direct or evanescent) and will be procured by UPV from outside the project.
- Proof of concept for the III-V O-band die onto SiN technology: UPV will carry the proof-of-concept of this technology over 150 mm silicon nitride patterned substrates by CSIC.

3 bullet points of action / objective for 2025Q4:

- UPV is scouting the market for O-band epi suppliers.
- Kick-off deferred to 2026Q2.

# T6.3 MTP of functional materials on thin SiPho (IMEC, TNI, UGENT) M6-M60

Objective: Extend imec SiPho PDK with heterogeneous building blocks

T6.3.1 electro-optic and magneto-optic bulk crystals (IMEC,UGent)

Action: develop process flow to obtain printable bulk crystal devices

T6.3.2 MTP of spotsize converters on imec SiPho (IMEC,UGent)

Action: installation of 3D printing tool for SSC definition on source wafer

T6.3.3 Micro-transfer printing of RGB laser diodes on imec SiPho (IMEC, UGent, TNI)

Action: define platform and integration strategy for RGB laser integration

T6.3.4 Maturing MTP of InP and LiNbO3 (IMEC,UGent)

Action: wafer-scale integration process development

T6.3.5 Alpha fab runs (IMEC,UGent,TNI)

No nearterm action

# T6.4 Hybrid PIC integration on thick Si (VTT, IMEC, CEA-LETI, SAL, TU/e, CSIC, UPV) M6-M60

Global objective: Development of hybrid integration of other PICs and components on VTT's 3 µm SOI PIC platform.

Critical and fundamental challenge: to realize highly efficient light coupling

- between 3 µm SOI waveguides and waveguides in other PICs:
- Further development of up-reflecting mirror (URM) process
- Develop GeSi based escalator process to replace a-Si escalators
- Develop high efficiency polymer writing based waveguide coupling solutions
- Develop low temperature flip-chip bonding process
- Develop micro transfer-printing (MTP) technology on thick SOI

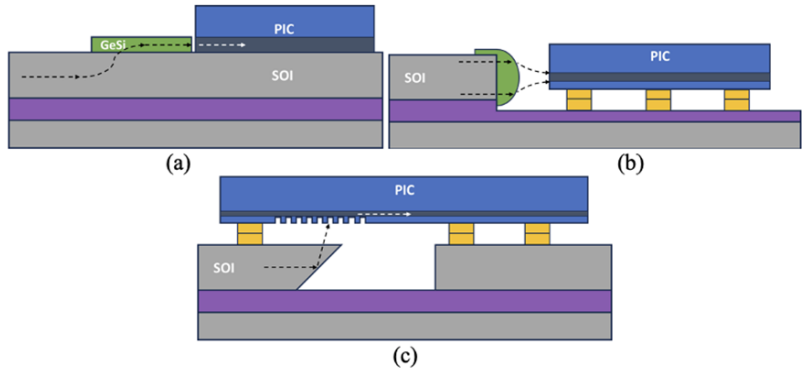



*Figure 29: Three approaches for hybrid integration interfaces on thick-SOI platform.*

Actions/objectives for 2025Q4:

- Thin film lithium niobate (TFLN) integration on thick SOI platform using waveguide escalator and flip-chip
- Preparing the epitaxial tool investment and tendering (in WP3)

| | Fabrication Technique | | | | | |
|---|---|---|---|---|---|---|
| **Monolithic PIC** | **MTP** | **LIFT** | **Flip-chip** | **Deposition** | **Growth** | **Wafer bonding** |
| **Thick Si** | III-V<br>TFLN<br><br>(Lasing, EO) | | III-V<br>Si<br><br>(Lasing, up-reflector) | | Ge/Si<br><br>(MIR applications) | |

# Placeholder for T6.5 (TNO)

# T6.6 Novel materials and functional layers for hybrid PICs (ICFO, SAL, UPV, WUT) M6-M60

- Main objective: investigate novel functional layers (TFLN, AlN, PCMs, PTMs, CQDs, UTMF) on Si, SiN, and Ge-on-Si platforms

- Description: study and development of all the steps needed to demonstrate the new hybrid platforms
  - substrate preparation
  - growth/deposition/transfer of functionalizing material
  - patterning of functionalized substrates
  - development of novel optical coupling strategies between substrate and functionalized layer
  - demonstration of new functionalities (modulation, light emission, detection, …)

- Objectives / Activities for 2025Q4: (M6-M7)
  - Definition of specific roles of partners involved in each hybrid platform
  - Define priority of approaches to be investigated for each hybrid platform based on state of the art
  - Define workflow, taking into account synergies between partners

# T6.7 Layered materials on monolithic PICS (UCAM, USOTON) M6-M60

**Main global objective**

1. Growth of graphene and related layered material (LM) over 8” wafers
2. Integration of LMs into PICs up to 8” scale and their characterization

**Brief description:**

1. Growth of high-quality, single-layer graphene and related layered materials on 200 mm (8 inch) wafers using an MOCVD system.
2. Preparation of PICs on 200 mm Si, SiN, and Ge-on-Si to build a layered-material (LM) hybrid integration platform (USOTON).
3. Transfer graphene onto PICs and cover it with materials like hBN or $WSe_2$ using wet or semi-dry transfer methods.
4. Characterization of graphene and based heterostructures using Raman, AFM, SEM after PIC integration.
5. Fabrication of graphene-based devices on PICs or on Si/SiNx test substrates, including Hall bars and TLM structures, to measure mobility and sheet resistance.

**Objective for 2025Q4**

- T6.7 will start at month 6, UCAM will coordinate with USOTON and other partners regarding wafer substrates exchange.

# Placeholder for T6.8 (CEA-LETI)

# T6.9 Photo-detector integration and control loop (POLIMI, FBK, CSIC) M6-M60

Global objective: Develop photodetectors (PDs), non-invasive optical power monitoring techniques and control loops into programmable photonic integrated circuits (PICs) for real-time monitoring, control, and reconfiguration.

Main Activities

- Si PIN PDs integrated into SiN PICs via evanescent coupling and backside thinning (FBK, CSIC).
- Development of SPAD detectors for 600–900 nm on SiNx platforms (FBK).
- Integrated (non-invasive) monitor PDs based on photo-resistive/photo thermal effects (POLIMI)
- Integration of Si-Ge detectors on SiC platform (POLIMI)
- Develop a control layer (electronics/software/algorithms) for automated calibration, configuration, and thermal stabilization (POLIMI) enabling tool for functional testing (Task T8.4)
- Contribution to optical/electrical I/O definition, integration with electronics, thermal management.

Activities for 2025Q4

- Present FBKs SPAD  PIN diode to WP partners
- Discuss with partners WP5 VIS waveguides  feasible architectures and integration schemes.
- Present integrated (non-invasive) monitor PDs for feedback and control. (POLIMI)

# T6.10 Plasma dicing of hybrid PICs on Si (UPV, CSIC, IMEC, UGENT, VTT, ICFO) M24-M60

Main global objective: development of plasma dicing process modules on Si substrate-based hybrid PIC platforms.

Brief description:

- Test & reliability technical comparison of incumbent vs new plasma dicing process.
- Technical comparison for silicon-only technologies.
- Technical comparison fo hybrid technologies.

3 bullet points of action / objective for 2025Q4:

- UPV is to prepare tenders for the capital equipment (plasma dicer).
- Kick-off deferred to 2026Q4.

# How to: monthly meeting, activity report

- Actions for task leading institutions (due for next WP6 meeting):
  - Task leading institution appoints task leader(s)
  - Partners name task participants and their roles
  - Task leader set-up regular meeting with task team (monthly)

- Monthly meeting + Activity report:
  - Each task 1-2 slides with a few bullet points on progress + next actions
  - Where it makes sense, a minimal timeline planning can be included
  - Tasks milestones to report: capital equipment install, new process, result (patent / publication)

  - Next monthly meeting is 16th of October 12:30 h CET

# AoB

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