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APPENDIX 6: ACTIVITIES LAUNCHED IN 2025 FOR THE CHIPS FOR EUROPE INITIATIVE PART

Version 6

CONTENTS

1 ACTIVITIES 2025 CHIPS FOR EUROPE INITIATIVE PART

This appendix foresees the launch of the following call topics with an estimated EU expenditure of as below:

HE ACTIONS		
Call Topics		
Topic	**Description**	**Indicative EU budget M€**
HORIZON-JU-Chips-2025-CSA	Pan-European infrastructure for Chips Design Innovation	**12**
HORIZON-JU-Chips-2025-IA-EDA	Open-source EDA tools development	**20**
Other actions not subject to calls for proposals		
HORIZON-JU-Chips-2025-RIA-SUP	Support for start-ups and SMEs	**220**
HORIZON-JU-Chips-2025-QAC1-1-SGA	Supporting developing Quantum Chip Technology for superconducting stability Pilot	**25**
HORIZON-JU-Chips-2025-QAC1-2-SGA	Supporting developing Quantum Chip Technology for photonic stability Pilot	**25**
HORIZON-JU-Chips-2025-QAC1-3-SGA	Supporting developing Quantum Chip Technology for semiconducting stability Pilot	**25**
HORIZON-JU-Chips-2025-QAC1-4-SGA	Supporting developing Quantum Chip Technology for diamond-based stability Pilot	**25**
HORIZON-JU-Chips-2025-QAC1-5-SGA	Supporting developing Quantum Chip Technology for neutral atoms stability Pilot	**25**
HORIZON-JU-Chips-2025-QAC2-SGA	Supporting developing Quantum Chip Technology for high-quality Trapped Ions Pilot	**25**
DEP ACTIONS		
Call Topics		
Topic	**Description**	**Indicative EU budget M€**
DIGITAL-JU-Chips-2025-CSA-DET	Set-up and integration of Design Enablement Teams	**5**
DIGITAL-Chips-2025-1-IA-LEAI	Low-power Edge AI Chips	**20**
DIGITAL-JU-Chips-2025-SG-SSOI	Accelerator for Advanced Strained Silicon on Insulator Substrates	**30**
DIGITAL-JU-Chips-2025-SG-LFA	Lab to Fab Accelerators for Advanced Packaging and heterogeneous integration	**50**
DIGITAL-JU-Chips-2025-CSA-LFA	Lab to Fab Accelerator ecosystem - Coordination and Support Actions. Boosting cooperation for industrial implementation on	**2**

	advanced packaging of chiplets and heterogeneous integration in Europe	
Other actions not subject to calls for proposals		
Topic	**Description**	**Indicative EU budget M€**
Call for tenders	Cloud platform for the European Design Platform	**15**
TOTAL		**424**

2 TECHNICAL DESCRIPTION OF THE CALL TOPICS

In addition to the application of Article 22(5) of the Horizon Europe Regulation[1] (HE) to the relevant topics of the Chips JU's work programme, in line with Article 23 of the Single Basic Act, in order to ensure a coherent application of Article 22(5) HE, as well as Union legislation and guidance application in similar topics in the work programme of the Chips JU, eligibility of participants in a proposal submitted to a Call for Proposals for any of the topics in this work programme will take into account any application of Article 22(5) of HE triggered for topics from other HE Work Programmes (including the Chips JU's work programme) for calls for proposals with similar scope. This may be of particular relevance to proposals submitted to bottom-up RIA/IA topics, i.c. topics HORIZON-JU-Chips-2025-IA and HORIZON-Chips-2025-RIA, where despite the fact that Article 22(5) HE might already be used, stricter conditions may apply in case those proposals address areas covered under other HE work programme topics with a stricter application of Article 22(5) HE.

2.1 Design Platform

Semiconductor circuit design involves the development of integrated circuits (ICs) and system-on-chips (SoCs) by defining the functionalities and specifications of chips, capturing a significant share of the value within the semiconductor supply chain. The industry is increasingly shifting towards more complex, application-specific, and highly integrated semiconductors, making state-of-the-art design essential for competitiveness and differentiation across various applications. In this evolving landscape, fabless companies are uniquely positioned to lead technological innovation and address the demands of diverse applications, further solidifying their critical role and driving growth within the semiconductor sector.

The Chips Act underscores the strategic importance of fostering chip design growth in Europe to enhance the competitiveness of the Union's semiconductor industry. Pillar I of the Chips Act, the Chips for Europe Initiative, outlines an ambitious plan to strengthen the Union's resilience in semiconductor technologies, including promoting the growth of fabless companies focused on leading-edge technologies. This is especially pertinent given that the European

[1] Regulation (EU) 2021/695 of the European Parliament and of the Council of 28 April 2021 establishing Horizon Europe – the Framework Programme for Research and Innovation, laying down its rules for participation and dissemination

share of global fabless semiconductor companies' revenues has shrunk to critically low levels, highlighting the urgent need for strategic initiatives to bolster this sector and enhance Europe's competitiveness. A critical mass of fabless companies is also key to generate further demand that would justify increased investment in semiconductor manufacturing capacity in Europe.

Recognising the Union's limited fabless capacity, and the significant barriers to entry in chip design, the Design Platform focuses on nurturing emerging companies in the sector. The Design Platform is at the heart of the Chips for Europe Initiative and is envisaged as a key instrument to foster the development of a strong design ecosystem in the Union by creating a pipeline of highly innovative European fabless companies, focusing particularly on the growth of start-ups and SMEs.

In 2024, the Chips Joint Undertaking launched a call for the selection of a Platform Coordination Team (PCT). The selected PCT should assist the Chips JU in defining the technical specifications of a cloud service for the platform to be procured by the Chips JU through a dedicated Call for Tenders. This cloud infrastructure should incorporate all the services necessary for the efficient implementation of the Design Platform including repositories, a user authentication service, license usage monitoring and any relevant *Infrastructure as Code* to be deployed at the various Design Enablement Teams (DETs).

The PCT will be complemented by a number of DETs that should set up a cloud-based environment for users designing on the platform, support them in their design cycle, and facilitate access of users to foundry services. Furthermore, the DETs should be responsible for providing access to foundry services. In fact, it should be a pre-requisite that for an entity to become a DET, it must act as, or be linked to, a foundry aggregator.[2]

These DETs may be design houses and RTOs with the necessary expertise and experience in providing such services. They can be spread geographically but may also have different sectoral (e.g. defence) or technological (e.g. digital, analogue, photonics) focus. The selection of DETs should take place via an open and inclusive process, based on fulfilment of certain technical and security requirements. Any design service provider fulfilling such requirements may apply for integration into the platform. The PCT should provide the set of requirements that DETs must fulfil in order to apply for integration in the cloud-based platform.
To this end this work programme includes the following topics:

- Cloud platform for the European Design Platform
- Set-up and integration of Design Enablement Teams
- Support to start-ups and SMEs.
- Open-source EDA tools development
- Low power Edge AI Chips

[2] A foundry aggregator is an industry standard term used for companies that act as an intermediary between fabless semiconductor companies (clients) and semiconductor foundries (manufacturers). Typically, only large enterprises directly engage with foundries.

2.1.1 Cloud platform for the European Design Platform

Type of Action	Call for tenders
Indicative EU budget (from the DEP budget)	15 M€
Mode	EU funding only

2.1.1.1 Context

Note: A formal call for tenders will be published over the course of 2025. The current text should not be considered as a formal Call for Tenders within the context of a procurement procedure. Information listed here is purely indicative.

Chip design is a key weakness in Europe's semiconductor ecosystem. Fabless revenues in Europe represent less than 1% of global revenues. Recognising the importance of this sector to the value chain, Pillar 1 of the Chips Act, the Chips for Europe Initiative foresees a design platform to enable start-ups and SMEs to venture in design. The Design Platform is foreseen to serve as a hub of services and resources for its users and to this end the Chips Joint Undertaking should procure a cloud infrastructure to enable the implementation of said platform. The cloud infrastructure should include both the underlying cloud service as well as any related development of custom software.

2.1.1.2 Scope

The central cloud infrastructure should host the IP, PDKs and open-source EDA tools as well as training services. This should be accompanied by a user authentication service. Interested parties should therefore be responsible for the provisioning and management of a secure and scalable cloud infrastructure capable of hosting these key elements of the Design Platform and its associated services. The selected service provider should be responsible for the setting up and maintenance of this service for 4 years.

This should be accompanied by a vendor-neutral software solution for automated infrastructure configuration, referred to here as Infrastructure as Code (IaC), to be deployed at the various Design Enablement Teams as part of a federated cloud infrastructure for the Design Platform. The purpose of this IaC should be to:

- **Standardise deployment**: The IaC should enable the Platform Coordination Team (PCT) to define and enforce a standardised configuration for DET cloud environments through code, ensuring that all DETs adhere to the same security protocols, service level agreements, and access controls. This would ensure a more consistent and reliable user experience across different DETs.
- **Automate provisioning**: The IaC related tools should be used to automate the provisioning of cloud resources for DETs. This would simplify the process of setting

up and scaling design environments, reducing the potential for manual errors and freeing up DET resources to focus on user support and other value-added services.

- **Ensure version control and reproducibility**: Through the IaC, the PCT should be able to leverage version control systems to track changes and ensure that environments can be easily reproduced. This should be crucial for maintaining consistency over time, simplifying troubleshooting, and facilitating the rollback of changes if needed.
- **Enhance security and compliance**: The IaC can help enforce security best practices by automating security configurations and checks. This could be particularly relevant for the DP, given the sensitive nature of design data and IP. By codifying security policies, the PCT could help ensure a more secure and compliant design environment for all users.

2.1.1.3 Expected outcomes.

The requested cloud services should primarily contain the following elements:

- A repository populated with an extensive portfolio of open-source and proprietary 'design assets' to facilitate and enhance the design process for users, such as intellectual property (IP) blocks, design templates, fast adoption kits, process design kits (PDKs) from pilot lines and open foundries, open-source design tools, as well as reusable open-access design elements from previous EU-funded projects.

- Any suitable features, such as user authentication and license usage monitoring, that are deemed useful for the management of the overall initiative and the various DETs in the Design Platform.

- Templates of virtual machines or containers containing all the software components and configuration required to operate a given electronic design software, and that can be easily deployed on the cloud instances operated by the DETs.

The selected tender should also be responsible for the running and maintenance of this service for 4 years.

The latter point should be complemented by the development of an *Infrastructure as Code* (IaC) framework that supports a variety of cloud vendors. Work related to the development and management of the IaC should be coordinated by the PCT and deployed across various DETs. The purpose of this IaC is to facilitate cloud deployment at the various DETs, ensure baseline security standards, and provide a consistent experience across different DETs. Where possible, cloud vendor-agnostic resources should be used, accompanied by vendor-specific configurations where necessary. The service of developing the IaC should also be procured by the Chips JU with the technical assistance of the PCT.

All resources involved in this development should be based in the EU, including the location of the cloud-related data centres.

Further details will be presented in the Call for Tenders when published.

2.1.2 Set-up and integration of Design Enablement Teams

Topic: DIGITAL-JU-Chips-2025-CSA-DET

Type of Action	CSA
Indicative EU budget	5 M€
Expected EU contribution per project	The JU estimates that an EU contribution of around EUR 0.5 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	EU funding only One stage Call with submission of Full Proposal (FPP)
Call launch date	*04th of June 2025*
Deadline FPP Phase	*30th of July 2025*

2.1.2.1 Context

Semiconductor circuit design is the process of creating integrated circuits (ICs) by defining the functionalities and characteristics of chips, capturing a substantial portion of the added value within the semiconductor value chain. The trend is moving towards more complex, application-specific, highly integrated semiconductors, making cutting-edge design crucial for competitiveness and differentiation in a wide range of applications. In this context, fabless semiconductor companies are well-positioned to drive technological advancements and meet the needs of diverse applications, reinforcing their pivotal role and growth in the semiconductor industry.

The Chips Act underscores the strategic importance of fostering chip design growth in Europe to enhance the competitiveness of the Union’s semiconductor industry. Pillar I of the Chips Act, the Chips for Europe Initiative, outlines an ambitious plan to strengthen the Union's resilience in semiconductor technologies, including promoting the growth of fabless semiconductor companies. This is especially pertinent given that the European share of global fabless semiconductor companies’ revenues has shrunk to critically low levels, highlighting the urgent need for strategic initiatives to bolster this sector and enhance Europe's competitiveness. A critical mass of fabless companies is also key to generate further demand that would justify increased investment in semiconductor manufacturing capacity in Europe.

The Design Platform is at the heart of the Chips for Europe Initiative. It is envisaged as a key instrument for fostering the development of a strong semiconductor design ecosystem in the Union, by supporting the growth of highly innovative European fabless start-ups and SMEs. Considering the Union’s limited fabless capacity, and the significant barriers to entry

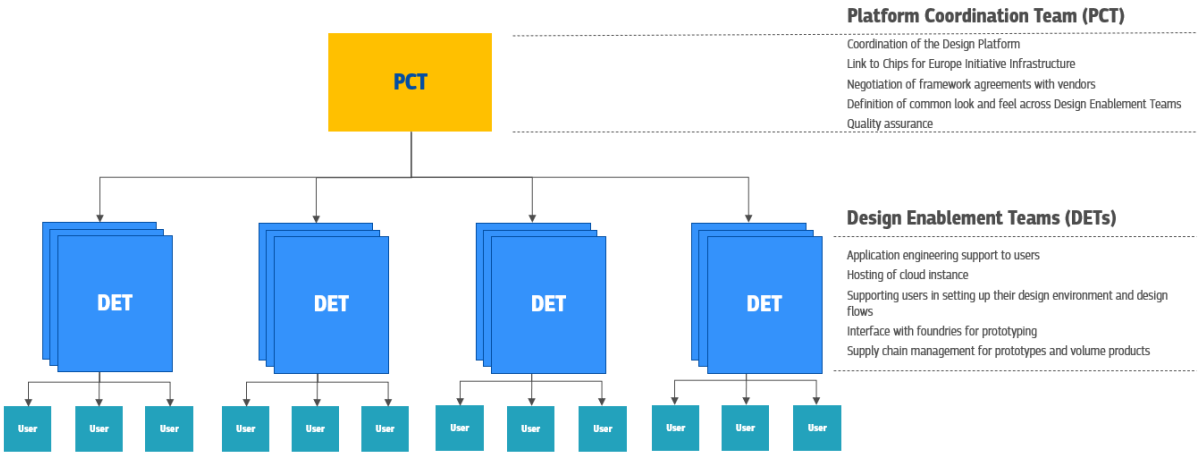
in chip design, the Design Platform will focus on nurturing emerging companies in the sector by enabling their access to a comprehensive chip design ecosystem from early stages up to tape-out.

This ecosystem includes a series of Electronic Design Automation (EDA) tools, Intellectual Property (IP) blocks and Process/Assembly Design Kits (P/ADKs) including standard cell libraries. This is coupled with either on-premise or cloud-based computing resources. Furthermore, access to foundries, packaging and test facilities is crucial. Each of these elements requires a separate acquisition process for the designer, often involving very significant costs and its own complex procedures.

2.1.2.2 Scope

The Design Platform should act as a hub of services to support European companies engaged in chip design. The Design Platform is implemented via two main classes of entities:

- The **Platform Coordination Team (PCT)** which coordinates the Design Platform, establishes framework agreements with EDA/IP suppliers and provides access to a central cloud service encompassing a marketplace with open source or proprietary IPs/EDA tools/PDKs and trainings amongst other resources. The PCT also provides DETs with Infrastructure as Code to ease the deployment of cloud instances. Through internal expertise and, where necessary, sub-contracting, the PCT and DETs collaborate to design and implement the overarching technical implementation of the platform and design interfaces with the distributed services, as well as ensuring the overall neutrality of the platform
- The **Design Enablement Teams (DETs)** each of which is in charge managing a distributed cloud instance and providing dedicated application engineering support to users from setting up their design environment and design flows up to tape-out. A DET can be a single entity, or a consortium of entities selected among providers of chips design support services, such as design houses, RTOs or other entities currently providing design enablement services on a commercial basis. DETs should be selected based on their technology expertise (e.g., digital, analogue, mixed-signal, photonics, etc.), ability to offer support across the end-to-end design flow, access to fabrication services (foundries, packaging, test services) and a proven track record of delivering high quality services to users, amongst other characteristics.



A call (*DIGITAL-Chips-2024-CSA-CDP-1*) to select a Platform Coordination Team was launched in July 2024. The scope of the current call is to select a number of Design Enablement Teams.

2.1.2.3 Expected outcomes.

The core functions of DETs include, but are not limited to:

1. **Deployment of Electronic Design Automation (EDA) tools on the cloud**: DETs will manage secured cloud instances facilitating access to essential design tools and simulation environments. To this end, DETs may contract with a cloud provider of their choice to setup this infrastructure.[3] It is expected that prospective DETs demonstrate experience in commercial designs using tools from established EDA vendors.
2. **Design flow support and customisation**: DETs will assist users in setting up and customising design environments and flows, ensuring smooth progression from initial setup to tape-out.
3. **Application engineering**: DETs will offer dedicated application engineering support, addressing specific user needs and challenges throughout the development process.
4. **Access to Process Design Kits (PDKs)**: DETs will provide users with access to the necessary PDKs and ADKs for their design projects. Each DET must have legal authorisation to use and/or provide its users access to PDKs/ADKs of at least one semiconductor foundry.
5. **Design expertise**: DETs will provide users with access to the necessary design expertise for their design projects, directly via the DET's resources and/or through partnerships with third parties.

[3] Cloud services utilised by the DET shall comply with robust cybersecurity security requirements such as the CEN/TS 18026:2024 standard or equivalent.

6. **Prototyping and fabrication services**: DETs will facilitate prototyping and fabrication services including packaging and testing through partnerships with leading foundries or aggregators, the Chips for Europe Initiative pilot lines or other relevant pilot lines. Each DET must have already established direct or indirect relationships with at least one semiconductor foundry, enabling efficient communication and ensuring technology advice and support to its users.

Overall, it is expected that each DET should manage a cloud instance offering dedicated application engineering support to users, from setting up their design environment and design flows to tape-out. The level of security of that cloud instance should be commensurate to the categories of users and applications that are expected to be running on this instance. The DET will maintain a cloud-based connection to the PCT's central cloud to manage user access, extend its capacity with additional resources (open-source IPs, EDA Tools, PDK...) and deliver periodic monitoring data to increase the quality of service of the Design Platform.

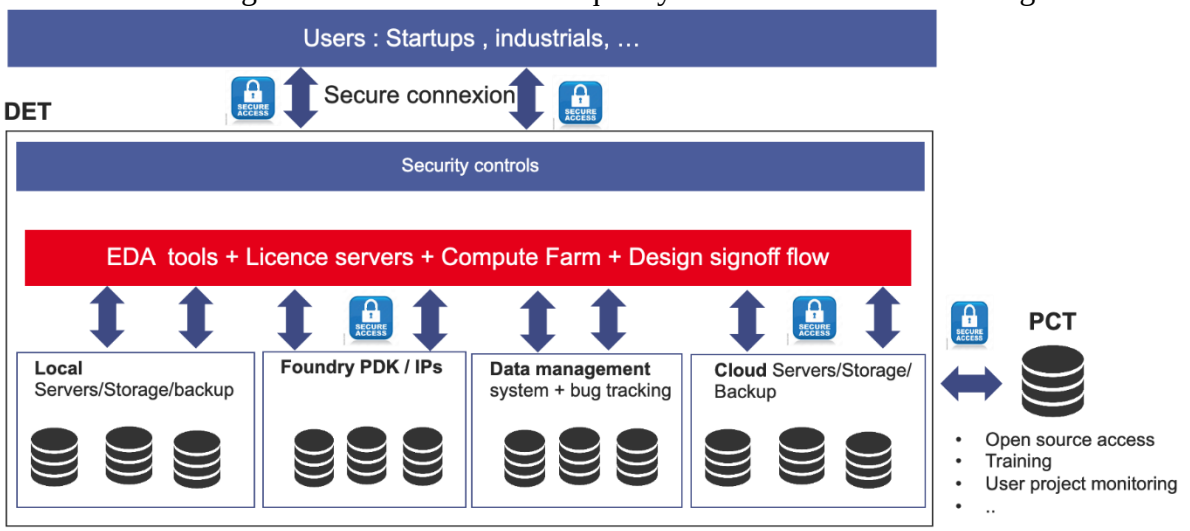


Figure 2 - High-level illustration of DET cloud-instance

DETs will be selected based on the extent of their technology expertise (e.g. digital, analogue, mixed-signal, photonics, etc.), ability to offer support across the end-to-end design flow, including PPA optimisation, access to fabrication services, and a proven track record of delivering high-quality services to users, among other characteristics.

These DETs could be public or private organisations that offer custom design support services, such as ASIC design houses and RTOs, with a demonstrated track record of expertise and experience in providing such services. Overall, the DETs should cover a wide variety of semiconductor technologies and can have different sectoral focuses (e.g. automotive, defence).

The only eligible costs for beneficiaries are those **directly related to the set-up and integration of DET's cloud services into the design platform**. This integration will be executed through a shared customer portal and the deployment of an Infrastructure as Code solution developed specifically for the Design Platform to ensure a consistent user experience.

The PCT will give access to these solutions to the designated DETs, for instance through an API. Any costs related to the infrastructure of the cloud provider of choice or through on-premise infrastructure, are considered to be part of the standard business proposition and competitive offering of the DET; as such, these costs are not considered eligible.

During the initial phase, the central cloud infrastructure of the design platform is likely to be still under development and thus not yet available for integration with the DET cloud service. Nevertheless, a preliminary trial phase of the design platform involving a limited set of test users may commence, and the selected DETs should be prepared to provide support and enablement services directly to such users from their own infrastructure, until the central platform becomes available for full service integration.

The selection process will ensure that collectively the selected DETs cover a broad range of technologies (CMOS and more than Moore technologies) and design topologies (analog, digital, mixed-signal etc.), for various applications (e.g. automotive, aeronautics, consumer, health etc). Preference will be given to DET candidates that address in their proposal at least one of the following technologies: CMOS bulk, FDSOI, finFET or Photonics. Strategies to collaborate with the Chips for Europe Initiative pilot lines are highly valued.

Proposals should provide a detailed explanation of the cloud services to be used by the DET, including their performance specifications and cybersecurity measures. Cloud services utilised by the DET should comply with robust cybersecurity requirements.[4]

DETs should also demonstrate capacity to effectively serve users across all the participating states of the Chips JU.

Finally, DET proposals which include members of the PCT consortium should clearly demonstrate effective measures to establish and maintain a strict separation between the two entities, including separate personnel and controlled communication channels, in order to ensure the full neutrality and independence of the PCT.

2.1.2.4 Admissibility

Admissibility conditions are described in Annex 2 “General DIGITAL EUROPE PROGRAMME conditions” of the WP General Annexes.

Regarding page limits:

- The page limit for the chapter RELEVANCE is 10 pages.
- The page limit for the chapter IMPLEMENTATION + chapter 4 of the template for the proposal (Part B) is 40 pages.
- The page limit for the chapter IMPACT is 10 pages.

[4] Such as the CEN/TS 18026:2024 standard or equivalent.

2.1.2.5 Eligibility

Eligibility conditions are described in Annex 2 of the WP General Annexes.
The following exceptions apply:

- Subject to participation restrictions for the protection of European digital infrastructures, communication and information systems, and related supply chains, as described in Annex 4 of the WP General Annexes.
- Legal entities that are established in the Union or EEA countries but are controlled from third countries may only participate on the condition that they guarantee the protection of the essential security interests of the Union and the Member States and that they ensure the protection of classified documents information. Where applicable, security guarantees need to be provided after proposal selection.

2.1.2.6 Financial and operational capacity and exclusion

Please refer to Annex 2 “General DIGITAL EUROPE PROGRAMME conditions” of the WP General Annexes.

2.1.2.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).
For the priority order of proposals with the same score, please refer to Annex 2 “General DIGITAL EUROPE PROGRAMME conditions” of the WP General Annexes.

2.1.2.8 Award criteria.

Please refer to Annex 2 “General DIGITAL EUROPE PROGRAMME conditions” of the WP General Annexes.

Specific rules may apply regarding the eligibility to national funding.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.1.2.9 Scores

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Relevance	0-5	1	3
Implementation	0-5	1	3

Impact	0-5	1	3
Total	0-15		10

(*) threshold applies to unweighted score.
(**) the weight is only used to establish the ranking of the proposals.

2.1.2.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to DIGITAL.

Type of beneficiary	**Maximum EU Contribution as % of eligible costs according to DIGITAL**
For profit organization but not an SME	100%
SME (for profit SME)	100 %
University/Other (not for profit)	100 %

2.1.3 Support for start-ups and SMEs

Topic: HORIZON-JU-Chips-2025-IA-SUP

Support to start-ups and SMEs making use of the Design Platform

Specific conditions	
Type of Action	Grant to identified beneficiary according to Financial Regulation Article 198 (f) – Innovation Action
Indicative EU budget	EUR 220 million.
Legal and financial set-up of the Grant Agreements	The rules are described in General Annex G of Horizon Europe Work Programme 2025[5]. The following exceptions apply: Beneficiaries may provide financial support to third parties. The support to third parties can only be provided in the form of grants. The EUR 60 000 threshold provided for in Article 207(a) of the Financial Regulation No 2024/2509 does not apply in order to be able to achieve the objectives of this action. The maximum amount of FSTP to be granted to an individual third party is EUR 8.1 million.
Mode	One stage, with submission of Full Project Proposal (FPP) FSTP recipients co-funded with NFA
Invitation date	03 December 2025
Deadline FPP	14 January 2026

2.1.3.1 Context

The Chips Act underscores the strategic importance of fostering the growth of chip design activities in Europe to enhance the competitiveness of the Union's semiconductor industry. Pillar I of the Chips Act, the Chips for Europe Initiative, outlines an ambitious plan to strengthen the Union's resilience in semiconductor technologies, also by promoting the growth of fabless startups. These fabless startups are key drivers of innovation, playing a crucial role in key sectors such as AI, telecommunications, and automotive.

[5] https://ec.europa.eu/info/funding-tenders/opportunities/docs/2021-2027/horizon/wp-call/2025/wp-14-general-annexes_horizon-2025_en.pdf

As fabless companies continue to drive growth in the semiconductor industry, the European share of global fabless semiconductor companies' revenues has shrunk to critically low levels. This highlights the urgent need for strategic initiatives to bolster this sector and enhance Europe's competitiveness. A critical mass of fabless companies is also key to generate further demand that would justify increased investment in semiconductor manufacturing capacity in Europe.

Currently, fabless start-ups can already find support in initiatives such as the Chips Fund, the Strategic Technologies for Europe Platform (STEP) programme, competence centres, and pilot lines. However, there is a crucial gap at the very early stages of these companies which the Design Platform seeks to address.

The Design Platform is at the heart of the Chips for Europe Initiative. It is a key instrument to foster the development of a strong design ecosystem in the Union by creating a pipeline of highly innovative European fabless companies. A key goal of the Design Platform is to support the growth of fabless companies by providing access to funding, foundries, design tools, IP and computing resources.

A consortium to manage the Design Platform, referred to as the Platform Coordination Team (PCT) was selected following a Call for Expression of Interest in Appendix 4 of the Chips Joint Undertaking Multiannual Work Programme 2023-2027. The same consortium was selected following a Call for Proposals for a Coordination and Support Action under Digital Europe in the aforementioned work programme. To ensure the overall coherence of the Platform, to give users a single point of contact, and considering its technical expertise, the consortium is expected to manage a start-up and SME support programme for early stage companies.

This action aims to add a particular aspect to the aforementioned support programme, the disbursement of grants, as well as potentially additional acceleration, incubation and other support activities catered to selected FSTP recipients.

2.1.3.2 Scope

Amongst others, the beneficiaries will be responsible for organising and implementing FSTP calls and their evaluations, administering the disbursement of grants and for additional support activities.

This programme will address a key gap in the support of early-stage start-ups and SMEs prior to commercialisation of their innovation. Supported third parties are expected to present innovative chip design projects with a clear perspective towards commercialisation. The programme will facilitate the scaling up of start-ups and SMEs engaged in chip design through FSTP grants.

The beneficiaries will collaborate with the providers of incubation and acceleration services that are funded via a Digital Europe grant for a Coordination and Support Action. The supported third parties will benefit from FSTP grants as well as incubation and acceleration services. In addition, the beneficiaries of this topic will work together with Design Enablement

Teams, who will provide dedicated application engineering support to users from setting up their design environment and design flows up to tape-outs.

Selections and Evaluation procedure to be run by the beneficiaries

Selections should be made by the beneficiaries with the assistance of a pool of independent experts that evaluate the proposals. Experts should be professionals from the field of semiconductor design or manufacturing and should have an understanding of both the technology and the semiconductor industry.

The criteria for giving the financial support for FSTP Level 1 must include the capacity of the applying third party to realise a proof-of-concept design, level of innovation, and EU added value. Beneficiaries are expected to further elaborate on these criteria.

The criteria for giving the financial support for FSTP Level 2 must include the quality of the business case, market viability of possible final products, the quality of the proof-of-concept demonstrator and designs, level of innovation, and EU added value. Beneficiaries are expected to further elaborate on these criteria.

The beneficiaries should establish a quick selection procedure to verify the eligibility of the third party and the capacity of the applying third party to realise a proof-of-concept design or a proof-of-concept demonstrator.

Scope for FSTP Level 1

The following applies to the selection of third parties receiving Level 1 services:

- Third parties should be invited to submit proposals for Level 1 services via a continuous application process with a number of cut-off dates determined by the consortium. There should be at least 2 cut-off dates per year during the continuous application period.
- Selected third parties must design the majority of their chips in-house, in the country of establishment.
- The maximum amount of financial support for Level 1 services should not exceed EUR 100 000 for each third party. A third party may only benefit from Level 1 services once; this includes linked entities.
- The exact amount of the financial support is based on estimates of the eligible costs given by the applicant and assessed by experts designated by the PCT. The funding rate will be up to 100%. Funding may be awarded in the form of lump sums. Funding is paid out based on reaching well-defined milestones. Prefinancing may be awarded as well.

Financial support for FSTP Level 1

Via FSTP calls, selected startups and SMEs may receive a grant covering certain pre-determined eligible costs.

- The financial support is granted to cover:

- Electronic Design Automation (EDA) tool license costs with vendors that have a "General Conditions Agreement" within the context of the Design Platform;
- semiconductor Intellectual Property (IP) blocks licence costs;
- DET services costs and/or costs related to access to computing resources;

Scope for FSTP Level 2

The following applies to the selection of third parties receiving Level 2 services:

- Third parties are invited to submit proposals for Level 2 services via a continuous application process with a number of cut-off dates determined by the consortium.[6] There should be at least 2 cut-off dates per year during the continuous application period.
- Selected third parties must design the majority of their chips in-house, in the country of establishment.
- The maximum amount of financial support for Level 2 services should not exceed EUR 8 000 000 for each third party. A third party may only benefit from Level 2 services once; this includes linked entities.
- The exact amount of the financial support is based on estimates of the eligible costs given by the applicant and assessed by experts designated by the PCT. The funding rate will be up to 35% Union funding, and may be complemented up to 70% by national and/or Union funding. Funding may be awarded in the form of lump sums. Funding is paid out based on reaching well-defined milestones. Prefinancing may be awarded as well.

Financial support for FSTP Level 2

Via FSTP calls, selected startups and SMEs may receive a grant covering certain pre-determined eligible costs.

Start-ups and SMEs in Level 2 may benefit from two main funding streams, provided from the Union's contribution and the Participating States' contribution.

- The financial support is granted to cover:
  - Electronic Design Automation (EDA) tool license costs with vendors that have a "General Conditions Agreement" within the context of the Design Platform;
  - semiconductor Intellectual Property (IP) blocks licence costs;
  - DET services costs and/or costs related to access to computing resources;
  - fabrication costs for prototyping.

[6] Prior use of Level 1 services is not a prerequisite for eligibility to apply for Level 2 services.

Admissibility for applications for FSTP

- Third parties should submit applications in a format defined by the PCT consortium. The complexity and length of the applications should be proportionate to the size of the grant.
- Proposals by third parties responding to FSTP calls should include:
    - a description and justification by the third party of the proposed costs;
    - evidence of the third party's financial capacity to carry out the proposed project, considering that a certain part of overall costs may need to be financed by the third party;
    - a description of the project as well as the professional experience of the third party;

Eligibility for start-ups and SMEs applying for FSTP

All organisations that are eligible for funding in Horizon Europe are eligible for funding in the FSTP calls organised by the beneficiaries. Recipients of FSTP grants will be granted access to the Design Platform[7].

For further conditions on financial support to third parties, proposers are referred to the Horizon Europe General Annexes[8].

In addition to eligibility to participate, for the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

2.1.3.3 Expected outcomes.

A main element of the Design Platform is a **start-up and SME incubation and acceleration programme** that is broadly based on two levels of support as seen in Figure 1.

This programme relies on the cloud service infrastructure managed by the PCT and procured by the Chips Joint Undertaking, as well as services provided by both the PCT and the Design Enablement Teams (DETs) following calls DIGITAL-Chips-2024-CSA-CDP-1 and DIGITAL-JU-Chips-2025-CSA-DET respectively.[9]

Within the context of this action, Level 1 services correspond to an incubation programme and Level 2 services correspond to an acceleration programme.

[7] It should be noted that previous work programmes (in particular, Annex 4 of the Chips JU's multi-annual work programme) provided other statements about access to the Design Platform. This has been corrected in the current work programme and in the access conditions specified in the Hosting Agreement, i.e., the formal agreement between the PCT consortium and the Chips JU that defines how the Design Platform is to be managed. It is therefore necessary to clarify here that recipients of FSTP grants will have access to the Design Platform and that all organisations eligible for Horizon Europe funding are also eligible for financial support under the FSTP calls of this topic.

[8] https://ec.europa.eu/info/funding-tenders/opportunities/docs/2021-2027/horizon/wp-call/2025/wp-14-general-annexes_horizon-2025_en.pdf

[9] As set out in Annexes 4 and 6 of the Chips Joint Undertaking's multi-annual work programme 2023-2027

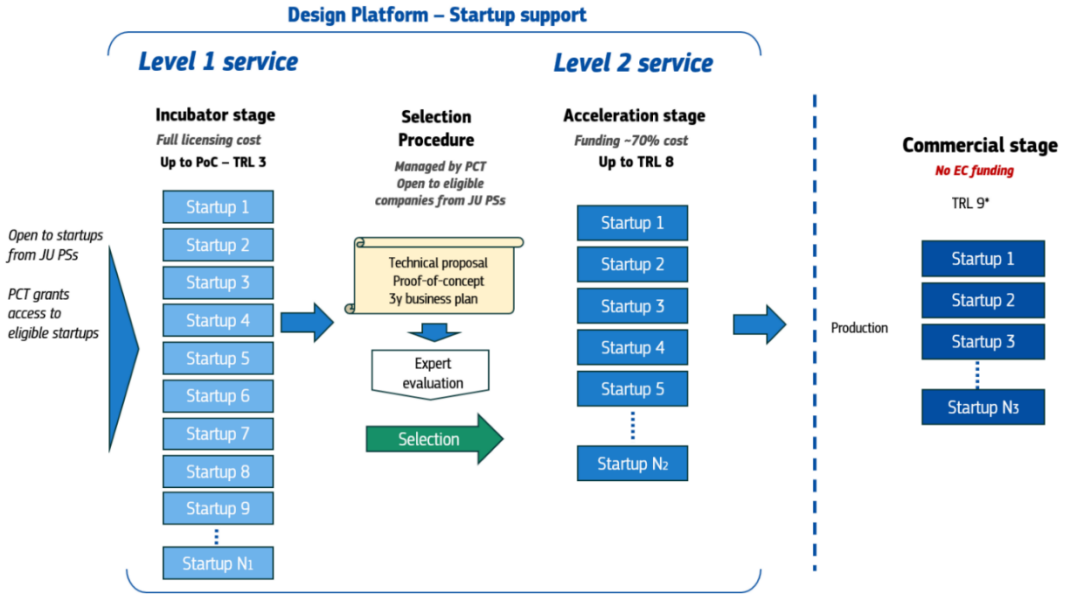


Figure 1 – Design Platform start-up and SME support programme

Beneficiaries need to ensure that Level 1 support is widely promoted and accessible to fabless European start-ups and SMEs. Here users will be given access to *proof-of-concept* licenses, IP and services that are usually subject to nominal fees. These fees will be partly financed via this action through grants to third parties. Level 1 support is primarily aimed at spinouts and early-stage start-ups.

Start-ups and SMEs at a more advanced stage of development may apply to a selection process to qualify for the Level 2 programme, which offers funding to cover up to 70% of the eligible costs for the selected companies. It is expected that the EU contribution provided via the PCT consortium plus national funding will cover up to 70% of eligible costs. It is expected that in the typical case the JU funding rate is up to 35%. The FSTP calls, including EU funding rates, should be discussed with the Chips JU before the opening of new and revised FSTP calls[10]. Here, EDA and IP license costs and/or conditions should be subject to a "General Conditions Agreement" or MoU agreed to by the Chips Joint Undertaking and made available to the Platform Coordination Team for users of the Design Platform.

Beneficiaries should ensure effective coordination with services and support activities for start-ups and SMEs financed by the Union outside of this action, particularly through the Coordination and Support Action (CSA) grant awarded to the DECIDE consortium acting as the Platform Coordination Team[11], to ensure that FSTP grantees are systematically monitored and supported.

[10] For administrative purposes, the maximum EU funding rate is considered to be 100%.
[11] Following a Call for Proposals in Annex 4 of the Chips Joint Undertaking's multi-annual work programme 2023-2027

The beneficiaries should demonstrate in their proposal the capacity to effectively organise and implement FSTP calls and their evaluations, to disburse grants to startups and SMEs, to assess performance of FSTP recipients, and to track progress over time.

Out of the total amount of EUR 220 million EU funding, the consortium is expected to commit at least 98% on financial support to third parties. At most 2% should be reserved to organise, evaluate, and manage FSTP calls, including awarding and monitoring and reviewing the execution of activities of FSTP recipients, and to execute other support activities. Incubation and acceleration services in addition to those funded via the Digital Europe grant for a Coordination and Support Action (CSA)[12] may be covered as well, if duly justified. Other activities, where deemed necessary for achieving the objectives of the topic, may be proposed as well. Support activities proposed need to be clearly delineated from those covered elsewhere.

Concretely, the following outcomes are expected:

- an effective and efficient start-up and SME support programme;
- a pipeline of sustainable fabless companies that have gone through an acceleration phase.

2.1.3.4 Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

Chapter	**FPP Phase**
Excellence	60 pages
Impact	100 pages
Quality and efficiency of the Implementation	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

[12] DIGITAL-Chips-2024-CSA-CDP-1 in Annex 4 of the Chips Joint Undertaking's multi-annual work programme 2023-2027

2.1.3.5 Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions (JU Grant):

Use of Article 198(f) of the Financial Regulation

Pursuant to Article 198(f) of the Financial Regulation, a grant may be awarded without a call for proposals for activities with specific characteristics that require a particular type of body on account of its technical competence, high degree of specialisation, or administrative powers, provided that the activities concerned do not fall within the scope of a call for proposals.

The DECIDE consortium acting as the Platform Coordination Team (PCT) and Hosting Consortium of the Design Platform following:

- a Call for Expression of Interest and a Digital Europe Call for Proposals in Appendix 4 of the Chips Joint Undertaking multiannual work programme 2023-2027 (REF: Chips-2024-CDP);
- evaluations by the Chips Joint Undertaking with the support of independent, suitably qualified experts; and
- selection and funding decisions by the Public Authorities Board of the Chips Joint Undertaking on the basis of a ranking list provided by independent experts;[13]

is deemed as the appropriate body to pursue this action in line with Article 198(f) of the Financial Regulation by fulfilling all the conditions required for the application of this provision, as set out below:

- The selected PCT consortium, *DECIDE*, is responsible for operating and coordinating all aspects of the Design Platform. This includes user onboarding and support, operation of the central cloud infrastructure, coordination of related design enablement services, and the implementation of mentoring, incubation, and acceleration programmes for start-ups and SMEs.
- Financial support to selected third parties, particularly start-ups and SMEs, making use of the Design Platform, as envisaged in this action, is a core feature of the Design Platform. Financial support for access to tools, IP, design enablement services and access to prototyping services is key to ensure that third parties can exploit the benefits provided by the deployed infrastructure.
- Annex C of the work programme[14] explicitly mandates that the selected "*PCT consortium shall be in charge of running a start-up incubation programme and a start-up acceleration programme in collaboration with the selected DETs*". Furthermore, the action corresponds to Phase 4 of the Design Platform's development, as outlined in

[13] Decision PAB 2024.56
[14] Appendix 4 Chips Joint Undertaking Multiannual Work Programme 2023-2027

Section 4.1.3 of the call for proposals REF Chips-2024-CDP-1,[15] under which the PCT consortium was selected. Section 4.1.3.2 of the call text explicitly makes clear that this phase involves providing support to start-ups and SMEs, complemented by contributions from Participating States.

- Due to the integrated nature of the Platform, this action requires tight coupling with the already ongoing activities of the PCT, financed through Chips-2024-CDP-1. Indeed, this action demands intricate knowledge of the Platform's architecture and user base, the ability to manage sensitive contractual arrangements with Electronic Design Automation (EDA) tool vendors negotiated by the PCT, and needs to be tightly coupled with the delivery of tailored support services to start-ups and SMEs. Via the PCT, start-ups and SMEs will have a single-point-of-contact for all services and support stemming from the Design Platform. Therefore, it would be inefficient for such activities to be executed by an entity independent of the PCT consortium.
- In addition, the DECIDE consortium will run a mentoring programme and already has the technical and organisational capacity to implement acceleration and incubation activities. Therefore, given that the DECIDE consortium is already funded via a grant to implement acceleration and incubation activities for all startups and SMEs, it is best placed to manage the complementary financial support to third parties participating in incubation and acceleration activities, as well as potentially additional acceleration, incubation and other support activities catered to selected FSTP recipients.

Furthermore, the activities covered by this invitation to submit a proposal represent a direct complement of work already entrusted to the PCT through a competitive procedure. This action is essential to the ongoing development and stability of the Design Platform. It is in line with Article 198(f) of the Financial Regulation and it is not within the scope of a call for proposals.

The PCT consortium is composed of the following legal entities:

1. INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM (IMEC), PIC 999981149, established in KAPELDREEF 75, LEUVEN 3001, Belgium, acting as the coordinator;
2. COMMISSARIAT A L'ENERGIE ATOMIQUE ET AUX ENERGIES ALTERNATIVES(CEA), PIC 999992401, established in RUE LEBLANC 25, PARIS 15 75015, France;
3. FRAUNHOFER GESELLSCHAFT ZUR FORDERUNG DER ANGEWANDTENFORSCHUNG EV (FHG), PIC 999984059, established in HANSASTRASSE 27C, MUNCHEN80686, Germany;
4. IHP GMBH - LEIBNIZ INSTITUTE FOR HIGH PERFORMANCEMICROELECTRONICS (IHP), PIC 999606438, established in IM TECHNOLOGIEPARK 25,FRANKFURT ODER 15236, Germany;
5. SILICON AUSTRIA LABS GMBH (SAL), PIC 901837907, established in SANDGASSE 34,GRAZ 8010, Austria;

[15] *Idem*

6. CENTRO ITALIANO PER IL DESIGN DEI CIRCUITI INTEGRATI ASEMICONDUTTORE (CHIPS-IT), PIC 878999548, established in VIA SANT'ENNODIO 26,PAVIA 27100, Italy;
7. AGENCIA ESTATAL CONSEJO SUPERIOR DE INVESTIGACIONES CIENTIFICAS(CSIC), PIC 999991722, established in CALLE SERRANO 117, MADRID 28006, Spain;
8. INTERNATIONAL IBERIAN NANOTECHNOLOGY LABORATORY (INL), PIC988145985, established in AVENIDA MESTRE JOSE VEIGA, BRAGA 4715-330, Portugal;
9. TECHNISCHE UNIVERSITEIT EINDHOVEN (TU/e), PIC 999977269, established in GROENE LOPER 3, EINDHOVEN 5612 AE, Netherlands;
10. TAMPEREEN KORKEAKOULUSAATIO SR (TAU), PIC 902999288, established in KALEVANTIE 4, TAMPERE 33100, Finland;
11. 11. CESKE VYSOKE UCENI TECHNICKE V PRAZE (CVUT), PIC 999848744, established in JUGOSLAVSKYCH PARTYZANU 1580/3, PRAHA 160 00, Czechia;
12. AKADEMIA GORNICZO-HUTNICZA IM. STANISLAWA STASZICA W KRAKOWIE(AGH), PIC 999844573, established in AL ADAMA MICKIEWICZA 30, KRAKOW 30-059, Poland;

A sub-set of the PCT consortium with selected legal entities from the ones above-mentioned may also be eligible for this call.

2.1.3.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 “HORIZON Europe conditions applicable to Chips JU” of the WP General Annexes.

2.1.3.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU.[16]

2.1.3.8 Award criteria

Award criteria are described in Annex 1 “HORIZON Europe conditions applicable to Chips JU” of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU. [17]

[16] Decision GB 2024.71
[17] *Idem*

2.1.3.9 Scores

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Relevance	0-5	1.0	3
Implementation	0-5	1.0	3
Impact	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

This is not related to anything. There are no such % in the FSTP or in the SUP

2.1.3.10 Reimbursement rate for establishing the EU contribution

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	Maximum EU Contribution as % of the Eligible Cost according to HE (*)
For profit organization but not an SME	70 %
SME (for profit SME)	70 %
University/Other (not for profit)	100 %

(*) beneficiaries may ask for a lower contribution.

On the maximum amount of financial support in line with Article 207(a) of the Financial Regulation

To achieve the objectives of this action, namely to provide start-ups and SMEs access to foundries, design tools, IP and computing resources, in line with the aims set out by the Chips Act, the maximum amount of financial support that can be paid to a third party must exceed the EUR 60.000 threshold set out in Article 207(a) of the Financial Regulation.

The nature of the costs related to the provision of Electronic Design Automation (EDA) tool licenses, IP licenses, foundry costs, computing resources and design enablement services, inherently surpass the threshold. As such, the objective of this action would be impossible to achieve without exceeding it.

Therefore, in accordance with paragraph 3 of Article 207(a) the threshold is exceeded and set at EUR 8.100.000.

2.1.4 Open-source EDA tools development

Topic: HORIZON-JU-Chips-2025-IA-EDA

Type of Action	Innovation Action (IA)
Indicative EU budget	20 M€
Expected EU contribution per project	The Chips JU estimates that an EU contribution of between EUR 6 and 7 million per project would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Two stage Call, with submission of Project Outline (PO) and Full Project Proposal (FPP)
Call launch date	04 March 2025
Deadline PO	29 Apr 2025 at 17:00 Brussels Time
Deadline FPP Phase	17 Sep 2025 at 17:00 Brussels Time

2.1.4.1 Context

A key objective of the Chips Act under the Chips for Europe Initiative is the 'building up of advanced design capacity for integrated semiconductor technologies'. To this end as part of operational objective 1 of the Chips Act, the Initiative should integrate 'new design facilities with extended libraries and electronic design automation (EDA) tools' into a virtual design platform. As part of a broader suite of resources, the Design Platform will make available a number of open-source tools.

Chip design is a vital element in the semiconductor value chain and open-source Electronic Design Automation (EDA) tools can be key drivers for innovation in this sector by enabling researchers and developers to experiment with new algorithms, architectures, and methodologies.

Access to EDA software, essential for chip development, has traditionally been both heavily restricted and prohibitively expensive, creating significant barriers for start-ups and small-to-medium-sized enterprises (SMEs). Open-source EDA tools can empower start-ups and SMEs with cost-efficient alternatives to expensive commercial licenses, allowing SMEs to

experiment with chip design. This is particularly crucial for SMEs operating in low- to mid-volume production.

Moreover, Europe is facing a considerable workforce shortage in this sector. This requires the cultivation of an open ecosystem to attract and develop more designers and developers. Open-source EDA tools lower the barrier of entry to chip design and thus attract new engineers and chip designers. Students and new entrants in the field can experiment with chip design without limitations on exploitation of their design or restrictive non-disclosure agreements (NDAs), fostering learning and experimentation. Therefore, wide-spread dissemination of these tools can help in addressing the skills gap in the semiconductor industry.

Existing open-source toolchains already support complete chip designs in several mature nodes, which are the technology of choice in a number of applications in fields such as radar design, automotive, aeronautics and space, medical technology, and electronics for harsh environments—industries with a strong European market presence. With relatively low tape-out costs, these nodes present minimal barriers for SMEs, and open-source tools could enable a wide array of European companies and start-ups to enter the chip design arena.

The growing accessibility of low-cost computing resources has opened the door for large-scale exploitation of parallel computing in EDA. However, this potential is often constrained by licensing costs, which limit the number of parallel runs needed for comprehensive adoption. This is an area where open-source implementations can be an interesting proposition. The ability to fully leverage computational resources for unrestricted parallel scaling—especially with the integration of modern machine learning technologies—has become a focal point of interest for many organisations seeking to push the boundaries of innovation.

Therefore, it is expected that over time, open-source EDA tools will offer significant benefits across other areas of chip design, including advanced nodes and highly integrated digital circuits, fostering growth and enhancing efficiency across the entire electronics sector.

The Horizon Europe *Go-IT* project[18] and the FOSSI Foundation have developed a roadmap for open-source hardware. This roadmap should be considered in proposals answering to this call.[19]

Proposals should, where relevant, build upon existing open-source resources and focus on advancing these tools to the next level. Efforts should include bridging the gap between open-source and commercial EDA tools - proposals should include a realistic outline with expectations and objectives to achieve this goal. Overall, proposals should include effective strategies for enhancing existing tools and improve user experience while driving innovation by introducing novel tools and methodologies. Where appropriate, machine learning techniques to improve performance and productivity should be considered.

[18] Go IT! | GOIT | Project | Fact sheet | HORIZON | CORDIS | European Commission
[19] Roadmap and Recommendations for Open Source EDA in Europe

Technology Readiness Level: Targeted TRL at the end of projects is between 7 and 8.

2.1.4.2 Scope

Each proposal must address only one of the following three streams: (i) digital SoC design; (ii) analogue and mixed-signal design; or (iii) productivity, interoperability, and verification. Only one project per stream will be selected.

(i) Digital SoC design

Modern integrated circuit (IC) design thrives on digital workflows and advanced design automation tools, enabling engineers to capitalise on the increasing circuit density achieved with each new technology node. The exponential progress driven by Moore's Law not only fuels innovation at the industry's forefront but also broadens accessibility across the technological landscape, including at more mature nodes. While much attention is given to cutting-edge design nodes, the enhanced productivity these advancements bring also empowers SMEs, even those with limited design expertise, to undertake projects previously beyond their reach. This democratisation of IC design opens up new markets, fosters innovation, and drives growth across the sector.

Digital chip design serves as the backbone for developing processors, memory, and logic components that power a vast array of electronic devices—from smartphones and computers to IoT systems and cutting-edge AI hardware. Currently, open-source EDA tools for digital design provide sufficient support for mature technology nodes. However, advancing to more sophisticated nodes requires refining existing tools and expanding their functionality. As technology nodes become smaller, the impact of parasitic effects on overall performance—both in terms of power and timing—grows significantly. Continued development is essential to accurately model and mitigate these effects.

(ii) Analogue and mixed-signal design

For stable, mature nodes, the availability of open-source Process Design Kits (PDKs) and comprehensive open-source design flows already provides significant opportunities for analogue and mixed-signal integrated circuit (IC) design. These tools are particularly valuable for education and training, enabling students, researchers, and engineers to gain hands-on experience in designing, manufacturing, and testing custom analogue and mixed-signal chips. By lowering the cost and accessibility barriers, these resources play a crucial role in equipping the next generation of designers with practical skills, particularly in fields such as sensors, communication systems, and signal processing.

Looking to the short-to-medium term, the goal is to achieve performance and reliability on par with proprietary tools while expanding the capabilities of open-source EDA solutions. Specific focus will be given to advancing tools and methodologies for complex analogue, radio frequency (RF), and terahertz (THz) designs, as these are essential for emerging technologies such as IoT, 5G/6G, and advanced communication systems. By prioritising analogue and

mixed-signal functionality from the outset, open-source EDA tools can drive innovation and expand access for this key segment of Europe's semiconductor ecosystem.

(iii) Productivity, interoperability, and verification

Addressing the challenge of labour shortages requires targeted measures to enhance efficiency and accessibility in chip design. In the short term, further developing and leveraging open-source tools can significantly boost productivity by reducing barriers to entry for engineers and designers.

In the short-to-medium term, focusing on improving interoperability between various Electronic Design Automation (EDA) tools will be crucial. Seamlessly integrating open-source EDA tools into established design workflows will enable smoother collaboration between diverse teams and disciplines. This interoperability will reduce time-consuming inefficiencies caused by incompatible systems, streamlining the design process from conceptualisation to final tape-out. For SMEs, in particular, this integration will lower technical barriers, making advanced chip design more accessible and cost-effective.

Furthermore, investing in open-source design verification tools will deliver benefits to the entire chip design industry. Fast and efficient verification solutions with minimal access barriers are essential for accelerating time-to-market and fostering wider adoption. In the medium term, the development of innovative verification methodologies will further enhance efficiency, streamline design processes, and attract skilled talent from diverse disciplines, addressing the industry's growing demand for expertise.

Such advancements will not only address immediate labour shortages but also strengthen the productivity of European SMEs in key industries, supporting their innovation in a rapidly evolving global market.

2.1.4.3 Expected outcomes.

Results stemming from this call should be well documented and widely disseminated. Precise documentation, user manuals as well as video tutorials should be made available. Selected consortia must develop teaching materials and courses with open resources and examples based on the developed/improved open-source EDA tools, accessible to academic institutions across the EU and suitable for self-study by individuals. To this end, collaboration with initiatives such as EUROPRACTICE is encouraged.

Consortia should actively engage with the Platform Coordination Team of the Chips Act's Design Platform to integrate their tools into the platform's design flows. Proposals must outline a clear strategy for engaging with relevant foundries to secure access to the required PDKs.

Proposals should clearly specify the applicable OSI-approved open-source license for all results. Proposals should also include a sustainability plan for results following the end of the project.[20]

[20] https://opensource.org/licenses

The three selected consortia should collaborate in their technical work where relevant. Joint communication and dissemination efforts are encouraged.

The expected outcomes for each of the aforementioned streams are the following:

(i) Digital SoC design

The overall ambition of this stream is to ensure a comprehensive and stable digital design flow in more mainstream nodes (65-28nm). Improvement of tools in more mature nodes is also within scope of this stream. To this end a baseline for the quality of results currently achievable with current state-of-the-art open-source tools needs to be determined.

The following outcomes should be considered:

- **Improved open-source EDA tools**: Achieved better result quality and performance of existing open-source EDA tools, especially for large-scale designs.
- **Optimised parasitic extraction workflow**: Delivered enhanced accuracy and efficiency in parasitic extraction, validated through experimental results on fabricated integrated circuits (ICs).
- **Industry-standard memory generators**: Developed high-quality memory generators for both mature and advanced technology nodes, meeting industry requirements.
- **Enhanced hierarchical design flows**: Strengthened support for hierarchical design methodologies and incremental build processes.
- **Timing and power analysis:** Robust tools for timing and power analysis for more advanced technology nodes.
- **Efficient SoC integration frameworks**: Provided streamlined frameworks for system-on-chip (SoC) integration, incorporating comprehensive verification support and design-for-test capabilities.
- **Open synthetic benchmark set:** Developed a publicly available synthetic benchmark set specifically designed for the evaluation and calibration of open EDA tools, facilitating improved performance analysis and comparison.
- **Open solutions for die-to-die communication**: Delivered open technological solutions for direct die-to-die communication, conforming to industry standards and incorporating the development of associated application development kits (ADKs).
- **Advanced tools for system-in-package design**: Developed cutting-edge tools to support system-in-package (SiP) designs.
- **Standardised interfaces for design tool interoperability**: Collaborated across streams to standardise interfaces between analogue, mixed-signal, and digital design tools, improving interoperability and simplifying design workflows.
- **Prototyped tapeouts for open-source tool validation**: Demonstrated tapeouts for mainstream and advanced nodes designed with open-source tools, enabling calibration and guiding mid- to long-term priorities.
- **Enhanced formal equivalence checking**: Improved the coverage and reliability of formal equivalence checking for critical elements of the design flow.

(ii) Analogue and mixed-signal design

The overall ambition of this stream is the development of a full analogue/mixed-signal design flow. The emphasis should extend beyond improving existing tools to include the adoption of innovative approaches and new paradigms.

The following outcomes should be considered:

- **High-performance analogue and mixed-signal simulators**: Delivered advanced analogue and mixed-signal simulation tools with efficient RF simulation capabilities, incorporating techniques such as shooting Newton analysis, harmonic balance analysis, transient noise simulation, and large-signal noise simulation.
- **Advanced electromagnetic simulation tools**: Developed state-of-the-art tools for electromagnetic (EM) simulations to support complex design needs.
- **Enhanced layout tools for parasitic extraction**: Achieved fast and accurate parasitic netlist extraction from large circuit layouts, incorporating netlist reduction techniques to improve efficiency.
- **Efficient custom layout generation tools**: Provided tools for efficient custom layout generation, combining programmatic approaches with AI-assisted manual layout capabilities.
- **Standardised interfaces for tool interoperability**: Collaborated across streams to standardise interfaces between analogue, mixed-signal, and digital design tools, ensuring improved interoperability and seamless workflow integration.
- **Robust EM simulation capabilities**: Delivered comprehensive EM simulation solutions with efficient data exchange between design entry tools and circuit simulators.
- **Curated tool collections and Integrated Design Environments**: Maintained and supported curated tool collections and integrated design environments, reducing barriers to entry and enabling standardised frameworks for IP generation.
- **Open-source IP generation frameworks**: Facilitated the creation of IP under open-source licence terms, including detailed documentation, verification test benches, and silicon validation results.

(iii) Productivity, interoperability, and verification

The overarching aim of this stream is to enhance productivity by adopting innovative design approaches and ensuring seamless data exchange between tools. This will be complemented by the development of robust verification processes that accommodate diverse methodologies and effectively tackle the increasing complexity of modern chip design.

The following outcomes should be considered:

- **High-speed mixed-mode simulation tools**: Delivered advanced simulation capabilities supporting both HDL or gate-level designs and analogue components for efficient mixed-mode analysis.
- **Tailored verification environments**: Enhanced verification tools and methodologies, creating robust environments specifically designed for analogue and mixed-signal designs.
- **Improved waveform viewing tools**: Developed enhanced waveform viewing tools with features such as automated waveform analysis, backtracing functionalities, and improved usability.

- **Standardised tool interfaces for interoperability**: Collaborated across streams to standardise interfaces between analogue, mixed-signal, and digital design tools, improving interoperability and streamlining design workflows.
- **Curated tool collections for IP generation**: Maintained and supported curated tool collections and integrated design environments, reducing barriers to entry and enabling standardised processes for IP creation and management.
- **Modular frameworks for design and verification**: Developed modular frameworks enabling custom integration of design and verification transformations.
- **Open data exchange guidelines**: Established requirements and guidelines for open data exchange formats to facilitate seamless communication between tools and systems.
- **Usability improvements for open-source EDA tools**: Implemented general usability and accessibility improvements to existing open-source EDA tools, meeting the needs of a diverse user base.
- **Support for industry-standard verification**: Provided robust support for industry-standard verification methodologies, integrating them with innovative verification technologies.
- **Cross-domain verification capabilities**: Enabled effective cross-domain verification across various abstraction levels, including hardware/software co-design.

2.1.4.4 Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.
Regarding page limits:

Chapter	PO Phase	FPP Phase
Excellence	60 pages	60 pages
Impact	60 pages	100 pages
Quality and efficiency of the Implementation	60 pages	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

2.1.4.5 Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Size limit	30 Participants
Max EU Contribution per partner (% of the total EU funding)	40%

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes).

Participation is limited to legal entities established in EU Member States, Norway, Iceland, Associated Countries, OECD and Mercosur countries (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed below, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

2.1.4.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

2.1.4.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.1.4.8 Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.1.4.9 Score

The scores will be given with a resolution of one decimal. The score table is for PO and FPP.

Criteria	Range	Weight (**)	Threshold (*)
Excellence	0-5	1.0	3
Impact	0-5	1.5	3
Quality and efficiency of the Implementation	0-5	0.7	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.1.4.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	Maximum EU Contribution as % of the Eligible Cost according to HE (*)
For profit organization but not an SME	20 %
SME (for profit SME)	30 %
University/Other (not for profit)	50 %

(*) beneficiaries may ask for a lower contribution.

2.1.5 A Pan-European infrastructure for Chips Design Innovation

Topic: HORIZON-JU-Chips-2025-CSA

Type of Action	Coordination and Support Actions (CSA)
Indicative EU budget	12 M€
Expected EU contribution per project	12 M€
Mode	EU funding only One stage Call, with submission of Full Project Proposal (FPP)
Call launch date	04 March 2025
Deadline FPP	29 Apr 2025 at 17:00 Brussels Time

2.1.5.1 Context

This call relates to the second general objective of the Chips JU: “build up large-scale design capacities for integrated semiconductor technologies”; and the seventh objective: “foster a dynamic Union-wide ecosystem based on digital value chains with simplified access to newcomers”, including the active involvement of Academia, RTOs, and SMEs. This call aims at supporting the follow-up, extension and consolidation of EUROPRACTICE services to provide Europe with an open-access platform to design and fabricate chips.

2.1.5.2 Expected Outcomes

Proposals are expected to address the following expected outcomes:

Here are the outcomes with the title capitalisation removed in the bold parts:

- **Establish a platform for the European design ecosystem**: Created a platform that supports the growth of a European design ecosystem by fostering design reuse, enabling the exploitation of advanced technologies in various application domains, and providing a foundation for deep-tech startups.
- **Encourage dissemination of PDKs through the platform**: Actively supported foundries in sharing open-source and proprietary technologies, particularly their PDKs, via the platform.
- **Streamline access to EDA tools**: Simplified and lowered barriers to access commercial and open-source industry-standard EDA tools across various technologies, with a focus on affordability.

- **Enhance workforce skills through hands-on experience**: Reduced barriers for undergraduate and postgraduate students to gain hands-on IC design experience, complementing their theoretical coursework.
- **Provide diverse chip design flows**: Offered a variety of chip design flows, supporting multi-vendor configurations where feasible, and assisted users in customising their design workflows.
- **Facilitate affordable prototyping access**: Enabled academia, research centres, and spinouts to prototype affordably using industrial-grade and emerging technologies, including advanced nodes, mature nodes, open-source solutions, and pilot-line technologies, with pathways to volume production.
- **Offer extensive training resources**: Delivered comprehensive training resources to up-skill and re-skill students and professionals across a wide range of technologies.
- **Train academics and instructors through 'train-the-trainer' programmes**: Provided targeted training for educators in semiconductor and photonics technologies to improve teaching quality and dissemination.
- **Provide a platform for open-source IP exchange**: Established a platform for sharing open-source IP, fostering collaboration and reuse.
- **Support students in gaining hands-on chip design experience**: Facilitated pre-tertiary and vocational students' access to open-source tool flows, promoting practical engagement with chip design.
- **Ensure access to customer support and leading-edge tools**: Simplified access to customer support, IP, and cutting-edge design tools for a broad user base.
- **Lower barriers for advanced packaging and integration**: Supported users in adopting advanced packaging and heterogeneous integration techniques by reducing entry barriers.
- **Enable efficient fabrication and system integration**: Facilitated multi-project wafer (MPW) runs and small-volume fabrication of ASICs, photonics, MEMS, sensors, and their integration at the system level, while promoting the adoption of emerging or underutilised technologies such as quantum technologies, photonics, and wide-bandgap materials by academia and SMEs.
- **Promote technology offerings from research centres**: Supported and highlighted the technology services of research centres with lower TRL (technology readiness level) capabilities.

    - Furthermore, particular emphasis should be placed on ensuring the seamless integration of this initiative within the framework of the Chips Act. To this end, proposals must address the following outcomes:

- Collaborate extensively with initiatives under Pillar 1 of the Chips Act such as the Design Platform, competence centres and pilot lines. Particularly by:
    i. collaborating extensively with the Design Platform initiative, including through joint activities;
    ii. facilitating academic access to the Chips Act pilot lines;
    iii. support competence centres across all EU Member States.
- Implement a comprehensive plan to **integrate EUROPRACTICE services into the Chips Act's Design Platform before the conclusion of this project**.

2.1.5.3 Scope

Semiconductors are at the centre of strong geostrategic interests, and at the core of the global technological race. A priority for Europe is to strengthen its design capacity and to lower the barriers to get access to advanced semiconductor technologies. Amongst others, this requires the nurturing and supply of people with the right digital skills, and the provision of routes to prototype and commercialisation. Not only large enterprises, but also startups and academic institutions play a key role and are crucial in the European semiconductor value chain.

Proposals need to lower the entry-barrier for academia, research institutes and very importantly for startups, and SMEs by offering affordable access to a portfolio of industrial-grade design tools, IP blocks, including open-source ones (e.g. RISC-V based), and prototyping technologies. Services offered must include initial advice, training, support, reduced entry costs, prototyping and a clear route to chip manufacture and product supply. Proposals should include a KPI on start-ups and SMEs that use the services provided by the platform.

Furthermore, proposals should include some of the following elements:

- Fostering collaboration and support in Europe by providing a design IP exchange system, where members can exchange IP blocks, including commercialisation of academic designs, considering national rules if relevant.
- Supporting and stimulating the adoption of emerging technologies (e.g. neuromorphic, 3D integration, wafer-scale-packaging etc) by creating standardised platforms and make those widely accessible;
- Enabling heterogeneous system integration, such as the adoption of chiplets by a wide range of customers.
- Strengthening industry relevant skills by supporting up-skilling and re-skilling initiatives through provision of extended training activities.
- Integrating the initiative into the broader framework of the Chips Act.

Reminding that of general importance to the Chips JU calls are:

- Re-use of results from previous ECSEL/Chips JU, H2020 or EUREKA-cluster projects is encouraged.
- Developing synergies with other relevant European, national or regional initiatives and/or funding programmes.
- Encouraging SMEs to participate in those developments, in particular paying attention to the needs of SMEs, involve SMEs in project execution, and develop solutions that can be taken up and/or exploited by SMEs.

In this topic the integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement.

2.1.5.4 Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

- The page limit for the chapter EXCELLENCE is 30 pages.
- The page limit for the chapter QUALITY AND EFFICIENCY OF THE IMPLEMENTATION is 30 pages.
- The page limit for the chapter IMPACT is 30 pages.

2.1.5.5 Eligibility

Applications will only be considered eligible if their content corresponds wholly (or at least in part) to the topic description for which they are submitted.

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes).

2.1.5.6 Financial and operational capacity and exclusion

Please refer to Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

2.1.5.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.1.5.8 Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.1.5.9 Score

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Excellence	0-5	1	3
Impact	0-5	1	3
Quality and efficiency of the Implementation	0-5	1	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.1.5.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to Horizon Europe.

Type of beneficiary	EU Contribution as % of the Eligible Cost according to HE
For profit organization but not an SME	100 %
SME (for profit SME)	100 %
University/Other (not for profit)	100 %

2.1.6 Low power Edge AI Chips

Topic: DIGITAL-Chips-2025-1-IA-LEAI

Type of Action	Simple Grant
Indicative EU budget	20 M€
Expected EU contribution per project	The JU estimates that an EU contribution of between EUR 4 and 5 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA One stage Call with submission of Full Proposal (FPP)
Call launch date	08 July 2025
Deadline FPP Phase	17 Sep 2025 at 17:00 Brussels Time

2.1.6.1 Expected Outcomes

Successful proposals are expected to deliver the following outcomes:

- Develop AI chip prototypes reaching TRL 6-7, integrating cutting-edge technologies such as non-volatile memories, neuromorphic computing, 3D heterogeneous integration, and photonic connectivity. These prototypes should be tested under real-world conditions and show potential for industrial scaling.
- Leverage the advanced capabilities of state-of-the-art infrastructures with fabrication and testing capabilities available within the Union, especially at leading Research and Technology Organisations (RTOs). This includes utilizing the Testing and Experimentation Facility (TEF) for Edge AI hardware (PREVAIL project[21]), a platform designed to accelerate the development of cutting-edge AI solutions, as well as Pilot Lines, including the ones of the Chips for Europe Initiative.
- The prototypes should demonstrate robust AI capabilities, including real-time inference, on-device learning, and adaptive decision-making. This enables edge AI

[21] https://prevail-project.eu/

systems to process data locally, make decisions, and adapt to changing environments without relying on cloud infrastructure, reducing latency and power consumption.

- The prototypes must achieve ultra-low power consumption to ensure energy-efficient AI operations in power-constrained edge environments, particularly for battery-powered devices. The emphasis should be on balancing computing power with energy efficiency.
- By advancing AI chips that are energy-efficient and highly secure, the developed technologies should contribute to Europe's digital transformation and help meet sustainability goals.

The ultimate goal of the project should be to drive the development of next-generation edge AI chips that combine high performance with ultra-low power consumption. These chips will enable real-time, on-chip AI capabilities for applications in fields like mobile communication networks (e.g. 6G), autonomous systems, industrial automation, and healthcare, all while aligning with Europe’s sustainability and digitalization goals.

2.1.6.2 Scope

Proposals to this call should target the development of next-generation edge AI chips, specifically delivering high-performance, ultra-low-power AI hardware solutions for applications at the edge of the network. The main scope should be to develop, test, and prototype next-generation edge AI technologies leveraging the advanced capabilities of state-of-the-art infrastructure available in the Union, such as the Testing and Experimentation Facility (TEF) for Edge AI hardware (PREVAIL project) as well as Pilot Lines, including the ones of the Chips for Europe Initiative. The objective is to accelerate the transition of advanced ultra-low power edge computing technologies “from the lab to the fab”, harnessing the facilities of leading European research and technology organizations.

The proposed edge AI chips should be based on technologies that overcome the memory bottlenecks of classical “Von Neumann” computing architecture, enabling substantial performance gains, including:

- Solutions for computing in-memory, using Non-Volatile Embedded Memories, such as Magnetoresistive Random Access Memory (MRAM), Oxide-based RAM (OxRAM), and Ferroelectric RAM (FeRAM) technologies. critical for achieving energy-efficient AI processing by enabling fast, low-power data storage and retrieval.
- Unconventional architectures for neuromorphic and analogue computing, mimicking the brain's neural networks by employing alternative AI approaches such as spiking neural networks (SNNs) artificial neural networks based on magnetic tunnel junctions (MTJ)and specialized materials, thereby enabling real-time on-chip sensing, learning and inference with extremely low energy overhead, drastically reducing power consumption.

- Advanced 3D integration and packaging technologies for the efficient integration of heterogeneous components (such as memory, computing, and I/O) into a single compact chip. By using interposer technologies, die-to-wafer, wafer-to-wafer, and Through-Silicon Via (TSV) techniques, chip prototypes can reduce the overall system footprint, improving performance and energy efficiency.
- Photonic Integrated Circuits (PICs) for ultrafast, energy-efficient artificial neural networks, enhancing both computational efficiency and data transfer speeds with low latency, ideal to ensure reliable high-speed connectivity in telecommunication networks and connected devices.

Proposals should target TRL 6-7 and demonstrate advancements in AI processing for real-time applications, while maintaining an emphasis on energy efficiency.

Consortia should be focussed on the realisation of the final prototype(s) and each partner should have a well-defined essential role towards the achievement of the objectives. Therefore, consortia are suggested to include strictly the participants that are required to cover the necessary tasks.

2.1.6.3 Admissibility

Admissibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Regarding page limits:

Chapter	PO Phase	FPP Phase
Relevance	60 pages	60 pages
Implementation	60 pages	100 pages
Impact	60 pages	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

2.1.6.4 Eligibility

Eligibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Specific eligibility conditions:

Size limit	70 Participants
Max EU Contribution per partner (% of the total EU funding)	50 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to participation restrictions for the protection of European digital infrastructures, communication and information systems, and related supply chains, as described in Annex 4 of the WP General Annexes.

Legal entities that are established in the Union or EEA countries but are controlled from third countries may only participate on the condition that they guarantee the protection of the essential security interests of the Union and the Member States and that they ensure the protection of classified documents information. Where applicable, security guarantees need to be provided after proposal selection.

2.1.6.5 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

2.1.6.6 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.1.6.7 Award criteria.

Please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes

Specific rules may apply regarding the eligibility to national funding.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.1.6.8 Scores

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Relevance	0-5	1.0	3

Implementation	0-5	1.0	3
Impact	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.1.6.9 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to DEP.

Type of beneficiary	**Maximum EU Contribution as % of the Eligible Cost according to DEP (*)**
For profit organization but not an SME	25 %
SME (for profit SME)	35 %
University/Other (not for profit)	35 %

(*) beneficiaries may ask for a lower contribution.

2.2 Accelerator for Advanced Strained Silicon on Insulator Substrates

Topic: DIGITAL-JU-Chips-2025-SG-SSOI

Type of Action	Simple Grant
Indicative EU budget	30 M€
Expected EU contribution per project	30 M€
Mode	Co-funded with the NFA One stage, with submission of Full Project Proposal (FPP)
Call launch date	08 Jul 2025
Deadline FPP	20 November 2025 at 17:00 Brussels Time

2.2.1.1 Context

The continuous demand for higher-performing, energy-efficient semiconductor devices is driving the need for innovation in substrate engineering. Industries such as telecommunications, automotive, and consumer electronics require advanced solutions that can meet the growing complexity of applications like 5G/6G communications, autonomous driving, and edge AI/ML computing. As conventional silicon technologies approach their physical limits in terms of speed, power efficiency, and miniaturisation, Strained Silicon on Insulator (sSOI) substrates are emerging as a key enabler of the next generation of semiconductor devices. By introducing strain into the silicon layer, sSOI enhances electron mobility, offering significant performance gains in advanced nodes such as 7nm FD-SOI.

FD-SOI technology is already a vital asset for Europe, offering an excellent balance between power consumption, speed, and cost. However, as the technology scales down to the 7nm node, integrating sSOI substrates becomes essential to maintain these advantages. The unique properties of sSOI effectively address the challenges posed by smaller transistor sizes, enabling improved energy efficiency and sustained high performance. This makes sSOI a crucial component in meeting the demands of Europe's key markets, including mobile and infrastructure, automotive sensors, and IoT devices.

To bridge the gap between research breakthroughs and industrial-scale production, there is an urgent need for a dedicated accelerator that can handle the complexities of sSOI substrate

development. Current R&D pilot lines lack the capacity and scale required to produce the thousands of wafers needed to ensure low defect densities and high manufacturing yields. An accelerator is essential to enable this transition, ensuring that sSOI substrates can meet the rigorous requirements for integration into advanced FD-SOI manufacturing processes.

This accelerator will provide the necessary infrastructure to validate sSOI substrates on an industrial scale, accelerating their adoption within the European semiconductor ecosystem. By supporting high-volume production, manufacturers can assess the feasibility and cost-effectiveness of sSOI in large-scale FD-SOI applications. This initiative will reinforce Europe's leadership in semiconductor innovation, ensuring the industry remains competitive in the global market for advanced devices.

Moreover, the accelerator will foster collaboration across the semiconductor value chain—from material providers to foundries and system integrators. This cooperation will reduce the risks associated with new substrate technologies and promote the rapid commercialization of sSOI-based solutions. In doing so, it will contribute to Europe's strategic goals of technological sovereignty and sustainability in key high-performance sectors.

2.2.1.2 Scope

The proposed accelerator should address all levels of the key technological steps required to bring sSOI substrates to industrial scale:

- **Development of industrial-grade sSOI substrates** will focus on achieving low defect density, crucial for enhancing electron mobility and ensuring high-performance FD-SOI devices at the 7 nm node. This will involve refining **strain engineering techniques**, particularly to introduce a uniform global strain that can balance the performance for strained NMOS and relaxed PMOS transistors.
- Ensure compatibility with existing semiconductor manufacturing, the accelerator will refine **process integration and optimisation**. This includes improving epitaxial growth, wafer bonding, and defect reduction techniques to meet the requirements of advanced FD-SOI production processes.

  Finally, the accelerator will **promote collaboration** across the semiconductor ecosystem, working with other pilot lines, as well as connecting to the design platform and competence centres, among others.

2.2.1.3 Expected Outcomes

The proposed accelerator should be established with all the necessary equipment and facilities, and will target the following main **objectives**:

- Develop **industrial-grade sSOI substrates** with reduced defect density to improve **electron mobility** and overall device performance. These substrates should be capable of addressing the market entry of 7nm FD-SOI expected by 2030 as well as be fully compatible with existing FD-SOI technologies, including 22FDX and 18nm FD-SOI.
- **Develop scalable and cost-effective manufacturing processes,** ensuring compatibility with current industrial standards and promoting widespread adoption.
- Demonstrate the feasibility of integrating **strained NMOS and relaxed PMOS areas**, balancing the performance of both transistors.
- Accelerate the transition from R&D to industrial-scale production by providing a pre-industrial infrastructure capable of **producing several thousand wafers per year**.
- **Develop demonstrators** to validate the benefits of sSOI-based FD-SOI over competing FinFET technologies, particularly in terms of improved RF performance, lower noise, and reduced power consumption.
- Enable open access to Process Design Kits (PDKs) and design building blocks to foster the differentiation of FD-SOI technology, including stress and relaxation design elements.
- Enable early-stage design and system-level integration of sSOI substrates through Multi-Project Wafer (MPW) runs, allowing timely validation of substrate performance in real-world applications. Support design efforts for high-speed broadband RF circuits, mm-Wave radar systems, and compact low power automotive and IoT solutions as part of the Next Gen FD-SOI roadmap.

The **expected results** for this accelerator should therefore comprise:

- Create a **sustainable accelerator open to all European stakeholders**, providing access to state-of-the-art sSOI technology and manufacturing capabilities.
- **Develop and standardize Process Design Kits** based on validated sSOI substrate data, enabling designers to optimise their system-level architectures and meet the demands of next-generation applications. These PDKs should support the transition to 7nm FD-SOI technology, ensuring readiness for high-volume manufacturing by 2030.
- Expand the capabilities of sSOI substrates to **industrial-scale wafer production**, ensuring low defect densities and improved manufacturing yields that meet the rigorous standards of advanced semiconductor fabrication.
- Drive the creation of **intellectual property** and strengthen Europe's production capacity in sSOI technologies, contributing to Europe's leadership in critical semiconductor markets.
- With a particular focus on complementarity with the FD-SOI pilot line, foster collaborative development through **synergies with other Chips JU pilot lines**, enhancing the overall innovation capacity and technological leadership of Europe in semiconductor technologies,

- Provide comprehensive **training programs and skill development** initiatives to equip European technologists and engineers with the expertise necessary for sSOI substrate integration and advanced semiconductor manufacturing.

2.2.1.4 Admissibility

Admissibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Regarding page limits:

Chapter	FPP Phase
Relevance	60 pages
Implementation	100 pages
Impact	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

2.2.1.5 Eligibility

Eligibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Specific eligibility conditions:

Size limit	70 Participants
Max EU Contribution per partner (% of the total EU funding)	50 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to participation restrictions for the protection of European digital infrastructures, communication and information systems, and related supply chains, as described in Annex 4 of the WP General Annexes.

Legal entities that are established in the Union or EEA countries but are controlled from third countries may only participate on the condition that they guarantee the protection of the

essential security interests of the Union and the Member States and that they ensure the protection of classified documents information. Where applicable, security guarantees need to be provided after proposal selection.

2.2.1.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

2.2.1.7 Evaluation procedure

For the specificity of each call evaluation please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.2.1.8 Award criteria.

Please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes

Specific rules may apply regarding the eligibility to national funding.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.2.1.9 Score

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Relevance	0-5	1.0	3
Implementation	0-5	1.0	3
Impact	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.2.1.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to DIGITAL.

Type of beneficiary	EU Contribution as % of the Eligible Cost according to DIGITAL (*)
For profit organization but not an SME	25 %
SME (for profit SME)	35 %
University/Other (not for profit)	35 %

(*) beneficiaries may ask for a lower contribution.

2.3 Quantum Chips

2.3.1 Supporting developing Quantum Chip Technology for superconducting stability Pilot

Topic: HORIZON-JU-Chips-2025-QAC1-1-SGA

Type of Action	RIA Specific grant agreement in relation to a Framework Partnership Agreement
Indicative EU budget	25 M€
Expected EU contribution per project	25 M€
Mode	Co-funded with the NFA One stage, with submission of Full Project Proposal (FPP)
Invitation date	30th July 2025
Deadline FPP	17th September 2025

2.3.1.1 Context

Within the Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots, the selected consortia will be invited to submit a proposal that will implement the first 3-4 years of the action plan for providing stable pilot fabrication capabilities defined in the FPA that would foster quantum chips production and rapid innovation tailored to meet the needs of the European quantum industry over the next decade, in particular start-ups and SMEs. The testing and experimentation facilities should be fully integrated in the pilots, providing seamless production and testing services.

2.3.1.2 Expected outcomes.

The proposal should aim to establish superconducting stability pilot production capabilities for a first of their kind quantum technology, where in the future European companies, research centres and academic institutions can produce quantum chips on a stable pilot scale based on a shared cost model between users and service providers. The targeted stability pilot should have a simple baseline process ready in 2-3 years from start of the project - reaching at least Technology Readiness Level (TRL) 6.

An early industrialization roadmap should be available by month 6 of the project, with the expectation that it will be regularly updated throughout the project's lifetime to incorporate evolving technical progress, market needs, and alignment with industrial partner requirements for scaling and commercialization towards mass production.

The proposal should focus on developing scalable production processes for quantum chips, with the goal of establishing industrial-level manufacturing methods. This includes the integration of cutting-edge Quantum Process Design Kits (PDKs) with the European Design Platform, aiming to standardize production workflows and minimize the need for custom developments. The proposal should include enabling technologies for quantum chips, namely advanced tools, components, and systems that facilitate the design, fabrication, operation, testing, and scaling of these devices. However, it should not include activities aimed at developing other essential components or subsystems that are unrelated or not directly integrated with the quantum chips. The initiative should seek to enhance technology and manufacturing readiness levels across the quantum industry, targeting applications in quantum computing, communications, simulations, and sensing. A key objective should be to establish standardized methodologies for the design, testing, and manufacturing of quantum chips, ensuring efficient production processes and broadening the range of applications in various sectors.

Key milestones should be clearly defined, with ambitious and technology-specific KPIs such as high yield, high-quality quantum chips, reliability, reproducibility, performance, and scalability of production. In addition, the proposal is expected to appropriately address the shortcomings identified in the Evaluation Summary Report of the corresponding FPA awarded under topic Chips-QAC-1, as appropriate to the relevant activities in the current SGA phase.

The proposal should demonstrate scalable, efficient, and stable production capabilities, with a focus on achieving high yield and consistency in quantum chip manufacturing. This will involve developing robust, repeatable manufacturing processes tailored to the unique requirements of superconducting quantum chips, ensuring a reliable supply chain for European stakeholders. Additionally, the proposal should outline the development of reliable characterization tools to ensure quality assurance, demonstrating the scalability of pilot technologies from small-to-mid volume fabrication to large-scale industrial production. A comprehensive technology roadmap and implementation plan should be defined to guide the industrialization of quantum chip production in the future and ensure the sustainability and growth of the quantum industry.

2.3.1.3 Scope

The action will require expertise in the area of manufacturing flows for quantum technologies, in particular in quantum computing/simulation (e.g. qubit fabrication), communication and sensing, and with issues regarding high-quality, reliability, versatility, process control including integrated testing and minimizing lead times. Interaction with standardisation bodies and data sharing on benchmarking is also encouraged.

The proposal should also cover: (i) the collaboration with other initiatives or programmes at regional, national, or European level such as Framework Partnership Agreements (FPAs) awarded under topic Chips-QAC-2: Call for establishing Framework Partnership Agreement(s) for developing Quantum Chip Technology for high-quality Stability Pilots, and the relevant Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots. This includes synergies and cooperation with the experimental pilot lines QU-PILOT and QU-TEST of the Quantum Flagship Initiative, for R&D support; (ii) any additional financial support they may receive in their activities from relevant national or regional initiatives.

In this topic the integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement.

2.3.1.4 Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

Chapter	**FPP Phase**
Excellence	60 pages
Impact	100 pages
Quality and efficiency of the Implementation	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

2.3.1.5 Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Max Contribution per partner (% of the total EU funding): 40 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details).

Participation is limited to legal entities established in EU Member States, Norway, Iceland, and Israel (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

2.3.1.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

2.3.1.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.1.8 Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.1.9 Score

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Excellence	0-5	1.0	3
Impact	0-5	1.0	3
Quality and efficiency of the Implementation	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.3.1.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	**Maximum EU Contribution as % of the Eligible Cost according to HE (*)**
For profit organization but not an SME	50 %
SME (for profit SME)	50 %
University/Other (not for profit)	50 %

(*) beneficiaries may ask for a lower contribution.

Purchases of equipment or other assets used for the action must be declared as depreciation costs. However, costs may exceptionally be declared as full capitalised costs for high-value equipment that is essential for the development of the pilots, particularly where such equipment contributes to the development of an EU ecosystem of equipment providers and users, and ultimately to European technological autonomy. This exception may apply where the equipment represents a significant share of the beneficiary's eligible costs and where limiting the cost to depreciation would introduce delays in the implementation or compromise project objectives. The list of eligible items to be declared as full capitalised costs, should be part of the proposal and will be confirmed by the Chips JU during the grant preparation process.

2.3.1.11 STEP and Sovereignty Seal

This topic contributes to the objectives of the *Strategic Technologies for Europe Platform* (STEP). As such, eligible proposals that exceed the evaluation thresholds will be awarded a *Sovereignty Seal*. The Sovereignty Seal is a quality label, valid for the duration of the project, which will facilitate access to additional EU funding (alternative, cumulative or combined funding from several EU budget instruments) or national public and private investments.

2.3.2 Supporting developing Quantum Chip Technology for photonic stability Pilot

Topic: HORIZON-JU-Chips-2025-QAC1-2-SGA

Type of Action	RIA Specific grant agreement in relation to a Framework Partnership Agreement
Indicative EU budget	25 M€
Expected EU contribution per project	25 M€
Mode	Co-funded with the NFA One stage, with submission of Full Project Proposal (FPP)
Invitation date	30th July 2025
Deadline FPP	17th September 2025

2.3.2.1 Context

Within the Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots, the selected consortia will be invited to submit a proposal that will implement the first 3-4 years of the action plan for providing stable pilot fabrication capabilities defined in the FPA that would foster quantum chips production and rapid innovation tailored to meet the needs of the European quantum industry over the next decade, in particular start-ups and SMEs. The testing and experimentation facilities should be fully integrated in the pilots, providing seamless production and testing services.

2.3.2.2 Expected outcomes.

The proposal should aim to establish photonic stability pilot production capabilities for a first of their kind quantum technology, where in the future European companies, research centres and academic institutions can produce quantum chips on a stable pilot scale based on a shared cost model between users and service providers. The targeted stability pilot should have a simple baseline process ready in 2-3 years from start of the project - reaching at least Technology Readiness Level (TRL) 6.

An early industrialization roadmap should be available by month 6 of the project, with the expectation that it will be regularly updated throughout the project's lifetime to incorporate

evolving technical progress, market needs, and alignment with industrial partner requirements for scaling and commercialization towards mass production.

The proposal should focus on developing scalable production processes for quantum chips, with the goal of establishing industrial-level manufacturing methods. This includes the integration of cutting-edge Quantum Process Design Kits (PDKs) with the European Design Platform, aiming to standardize production workflows and minimize the need for custom developments. The proposal should include enabling technologies for quantum chips, namely advanced tools, components, and systems that facilitate the design, fabrication, operation, testing, and scaling of these devices. However, it should not include activities aimed at developing other essential components or subsystems that are unrelated or not directly integrated with the quantum chips. The initiative should seek to enhance technology and manufacturing readiness levels across the quantum industry, targeting applications in quantum computing, communications, simulations, and sensing. A key objective should be to establish standardized methodologies for the design, testing, and manufacturing of quantum chips, ensuring efficient production processes and broadening the range of applications in various sectors.

Key milestones should be clearly defined, with ambitious and technology-specific KPIs such as high yield, high-quality quantum chips, reliability, reproducibility, performance, and scalability of production. In addition, the proposal is expected to appropriately address the shortcomings identified in the Evaluation Summary Report of the corresponding FPA awarded under topic Chips-QAC-1, as appropriate to the relevant activities in the current SGA phase.

The proposal should demonstrate scalable, efficient, and stable production capabilities, with a focus on achieving high yield and consistency in quantum chip manufacturing. This will involve developing robust, repeatable manufacturing processes tailored to the unique requirements of photonic quantum chips, ensuring a reliable supply chain for European stakeholders. Additionally, the proposal should outline the development of reliable characterization tools to ensure quality assurance, demonstrating the scalability of pilot technologies from small-to-mid volume fabrication to large-scale industrial production. A comprehensive technology roadmap and implementation plan should be defined to guide the industrialization of quantum chip production in the future and ensure the sustainability and growth of the quantum industry.

2.3.2.3 Scope

The action will require expertise in the area of manufacturing flows for quantum technologies, in particular in quantum computing/simulation (e.g. qubit fabrication), communication and sensing, and with issues regarding high-quality, reliability, versatility, process control including integrated testing and minimizing lead times. Interaction with standardisation bodies and data sharing on benchmarking is also encouraged.

The proposal should also cover: (i) the collaboration with other initiatives or programmes at regional, national, or European level such as Framework Partnership Agreements (FPAs) awarded under topic Chips-QAC-2: Call for establishing Framework Partnership Agreement(s)

for developing Quantum Chip Technology for high-quality Stability Pilots, and the relevant Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots. This includes synergies and cooperation with the experimental pilot lines QU-PILOT and QU-TEST of the Quantum Flagship Initiative, for R&D support; (ii) any additional financial support they may receive in their activities from relevant national or regional initiatives.

In this topic the integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement.

2.3.2.4 Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

Chapter	**FPP Phase**
Excellence	60 pages
Impact	100 pages
Quality and efficiency of the Implementation	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

2.3.2.5 Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Max Contribution per partner (% of the total EU funding): 40 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details).

Participation is limited to legal entities established in EU Member States, Norway, Iceland, and Israel (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

2.3.2.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

2.3.2.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.2.8 Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.2.9 Score

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Excellence	0-5	1.0	3
Impact	0-5	1.0	3
Quality and efficiency of the Implementation	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.3.2.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	**Maximum EU Contribution as % of the Eligible Cost according to HE (*)**
For profit organization but not an SME	50 %
SME (for profit SME)	50 %
University/Other (not for profit)	50 %

(*) beneficiaries may ask for a lower contribution.

Purchases of equipment or other assets used for the action must be declared as depreciation costs. However, costs may exceptionally be declared as full capitalised costs for high-value equipment that is essential for the development of the pilots, particularly where such equipment contributes to the development of an EU ecosystem of equipment providers and users, and ultimately to European technological autonomy. This exception may apply where the equipment represents a significant share of the beneficiary's eligible costs and where limiting the cost to depreciation would introduce delays in the implementation or compromise project objectives. The list of eligible items to be declared as full capitalised costs must be part of the proposal and will be confirmed by the Chips JU during the grant preparation process.

2.3.2.11 STEP and Sovereignty Seal

This topic contributes to the objectives of the *Strategic Technologies for Europe Platform* (STEP). As such, eligible proposals that exceed the evaluation thresholds will be awarded a *Sovereignty Seal*. The Sovereignty Seal is a quality label, valid for the duration of the project, which will facilitate access to additional EU funding (alternative, cumulative or combined funding from several EU budget instruments) or national public and private investments.

2.3.3 Supporting developing Quantum Chip Technology for semiconducting stability Pilot

Topic: HORIZON-JU-Chips-2025-QAC1-3-SGA

Type of Action	RIA Specific grant agreement in relation to a Framework Partnership Agreement
Indicative EU budget	25 M€
Expected EU contribution per project	25 M€
Mode	Co-funded with the NFA One stage, with submission of Full Project Proposal (FPP)
Invitation date	30th July 2025
Deadline FPP	17th September 2025

2.3.3.1 Context

Within the Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots, the selected consortia will be invited to submit a proposal that will implement the first 3-4 years of the action plan for providing stable pilot fabrication capabilities defined in the FPA that would foster quantum chips production and rapid innovation tailored to meet the needs of the European quantum industry over the next decade, in particular start-ups and SMEs. The testing and experimentation facilities should be fully integrated in the pilots, providing seamless production and testing services.

2.3.3.2 Expected outcomes.

The proposal should aim to establish semiconducting stability pilot production capabilities for a first of their kind quantum technology, where in the future European companies, research centres and academic institutions can produce quantum chips on a stable pilot scale based on a shared cost model between users and service providers. The targeted stability pilot should have a simple baseline process ready in 2-3 years from start of the project - reaching at least Technology Readiness Level (TRL) 6.

An early industrialization roadmap should be available by month 6 of the project, with the expectation that it will be regularly updated throughout the project's lifetime to incorporate

evolving technical progress, market needs, and alignment with industrial partner requirements for scaling and commercialization towards mass production.

The proposal should focus on developing scalable production processes for quantum chips, with the goal of establishing industrial-level manufacturing methods. This includes the integration of cutting-edge Quantum Process Design Kits (PDKs) with the European Design Platform, aiming to standardize production workflows and minimize the need for custom developments. The proposal should include enabling technologies for quantum chips, namely advanced tools, components, and systems that facilitate the design, fabrication, operation, testing, and scaling of these devices. However, it should not include activities aimed at developing other essential components or subsystems that are unrelated or not directly integrated with the quantum chips. The initiative should seek to enhance technology and manufacturing readiness levels across the quantum industry, targeting applications in quantum computing, communications, simulations, and sensing. A key objective should be to establish standardized methodologies for the design, testing, and manufacturing of quantum chips, ensuring efficient production processes and broadening the range of applications in various sectors.

Key milestones should be clearly defined, with ambitious and technology-specific KPIs such as high yield, high-quality quantum chips, reliability, reproducibility, performance, and scalability of production. In addition, the proposal is expected to appropriately address the shortcomings identified in the Evaluation Summary Report of the corresponding FPA awarded under topic Chips-QAC-1, as appropriate to the relevant activities in the current SGA phase.

The proposal should demonstrate scalable, efficient, and stable production capabilities, with a focus on achieving high yield and consistency in quantum chip manufacturing. This will involve developing robust, repeatable manufacturing processes tailored to the unique requirements of semiconducting quantum chips, ensuring a reliable supply chain for European stakeholders. Additionally, the proposal should outline the development of reliable characterization tools to ensure quality assurance, demonstrating the scalability of pilot technologies from small-to-mid volume fabrication to large-scale industrial production. A comprehensive technology roadmap and implementation plan should be defined to guide the industrialization of quantum chip production in the future and ensure the sustainability and growth of the quantum industry.

2.3.3.3 Scope

The action will require expertise in the area of manufacturing flows for quantum technologies, in particular in quantum computing/simulation (e.g. qubit fabrication), communication and sensing, and with issues regarding high-quality, reliability, versatility, process control including integrated testing and minimizing lead times. Interaction with standardisation bodies and data sharing on benchmarking is also encouraged.

The proposal should also cover: (i) the collaboration with other initiatives or programmes at regional, national, or European level such as Framework Partnership Agreements (FPAs) awarded under topic Chips-QAC-2: Call for establishing Framework Partnership Agreement(s)

for developing Quantum Chip Technology for high-quality Stability Pilots, and the relevant Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots. This includes synergies and cooperation with the experimental pilot lines QU-PILOT and QU-TEST of the Quantum Flagship Initiative, for R&D support; (ii) any additional financial support they may receive in their activities from relevant national or regional initiatives.

In this topic the integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement.

2.3.3.4 Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

Chapter	**FPP Phase**
Excellence	60 pages
Impact	100 pages
Quality and efficiency of the Implementation	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

2.3.3.5 Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Max Contribution per partner (% of the total EU funding): 40 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details).

Participation is limited to legal entities established in EU Member States, Norway, Iceland, and Israel (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

2.3.3.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

2.3.3.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.3.8 Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.3.9 Score

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Excellence	0-5	1.0	3
Impact	0-5	1.0	3
Quality and efficiency of the Implementation	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.3.3.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	**Maximum EU Contribution as % of the Eligible Cost according to HE (*)**
For profit organization but not an SME	50 %
SME (for profit SME)	50 %
University/Other (not for profit)	50 %

(*) beneficiaries may ask for a lower contribution.

Purchases of equipment or other assets used for the action must be declared as depreciation costs. However, costs may exceptionally be declared as full capitalised costs for high-value equipment that is essential for the development of the pilots, particularly where such equipment contributes to the development of an EU ecosystem of equipment providers and users, and ultimately to European technological autonomy. This exception may apply where the equipment represents a significant share of the beneficiary's eligible costs and where limiting the cost to depreciation would introduce delays in the implementation or compromise project objectives. The list of eligible items to be declared as full capitalised costs must be part of the proposal and will be confirmed by the Chips JU during the grant preparation process.

2.3.3.11 STEP and Sovereignty Seal

This topic contributes to the objectives of the *Strategic Technologies for Europe Platform* (STEP). As such, eligible proposals that exceed the evaluation thresholds will be awarded a *Sovereignty Seal*. The Sovereignty Seal is a quality label, valid for the duration of the project, which will facilitate access to additional EU funding (alternative, cumulative or combined funding from several EU budget instruments) or national public and private investments.

2.3.4 Supporting developing Quantum Chip Technology for diamond-based stability Pilot

Topic: HORIZON-JU-Chips-2025-QAC1-4-SGA

Type of Action	RIA Specific grant agreement in relation to a Framework Partnership Agreement
Indicative EU budget	25 M€
Expected EU contribution per project	25 M€
Mode	Co-funded with the NFA One stage, with submission of Full Project Proposal (FPP)
Invitation date	30th July 2025
Deadline FPP	17th September 2025

2.3.4.1 Context

Within the Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots, the selected consortia will be invited to submit a proposal that will implement the first 3-4 years of the action plan for providing stable pilot fabrication capabilities defined in the FPA that would foster quantum chips production and rapid innovation tailored to meet the needs of the European quantum industry over the next decade, in particular start-ups and SMEs. The testing and experimentation facilities should be fully integrated in the pilots, providing seamless production and testing services.

2.3.4.2 Expected outcomes.

The proposal should aim to establish diamond-based stability pilot production capabilities for a first of their kind quantum technology, where in the future European companies, research centres and academic institutions can produce quantum chips on a stable pilot scale based on a shared cost model between users and service providers. The targeted stability pilot should have a simple baseline process ready in 2-3 years from start of the project - reaching at least Technology Readiness Level (TRL) 6.

An early industrialization roadmap should be available by month 6 of the project, with the expectation that it will be regularly updated throughout the project's lifetime to incorporate

evolving technical progress, market needs, and alignment with industrial partner requirements for scaling and commercialization towards mass production.

The proposal should focus on developing scalable production processes for quantum chips, with the goal of establishing industrial-level manufacturing methods. This includes the integration of cutting-edge Quantum Process Design Kits (PDKs) with the European Design Platform, aiming to standardize production workflows and minimize the need for custom developments. The proposal should include enabling technologies for quantum chips, namely advanced tools, components, and systems that facilitate the design, fabrication, operation, testing, and scaling of these devices. However, it should not include activities aimed at developing other essential components or subsystems that are unrelated or not directly integrated with the quantum chips. The initiative should seek to enhance technology and manufacturing readiness levels across the quantum industry, targeting applications in quantum computing, communications, simulations, and sensing. A key objective should be to establish standardized methodologies for the design, testing, and manufacturing of quantum chips, ensuring efficient production processes and broadening the range of applications in various sectors.

Key milestones should be clearly defined, with ambitious and technology-specific KPIs such as high yield, high-quality quantum chips, reliability, reproducibility, performance, and scalability of production. In addition, the proposal is expected to appropriately address the shortcomings identified in the Evaluation Summary Report of the corresponding FPA awarded under topic Chips-QAC-1, as appropriate to the relevant activities in the current SGA phase.

The proposal should demonstrate scalable, efficient, and stable production capabilities, with a focus on achieving high yield and consistency in quantum chip manufacturing. This will involve developing robust, repeatable manufacturing processes tailored to the unique requirements of diamond-based quantum chips, ensuring a reliable supply chain for European stakeholders. Additionally, the proposal should outline the development of reliable characterization tools to ensure quality assurance, demonstrating the scalability of pilot technologies from small-to-mid volume fabrication to large-scale industrial production. A comprehensive technology roadmap and implementation plan should be defined to guide the industrialization of quantum chip production in the future and ensure the sustainability and growth of the quantum industry.

2.3.4.3 Scope

The action will require expertise in the area of manufacturing flows for quantum technologies, in particular in quantum computing/simulation (e.g. qubit fabrication), communication and sensing, and with issues regarding high-quality, reliability, versatility, process control including integrated testing and minimizing lead times. Interaction with standardisation bodies and data sharing on benchmarking is also encouraged.

The proposal should also cover: (i) the collaboration with other initiatives or programmes at regional, national, or European level such as Framework Partnership Agreements (FPAs) awarded under topic Chips-QAC-2: Call for establishing Framework Partnership Agreement(s)

for developing Quantum Chip Technology for high-quality Stability Pilots, and the relevant Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots. This includes synergies and cooperation with the experimental pilot lines QU-PILOT and QU-TEST of the Quantum Flagship Initiative, for R&D support; (ii) any additional financial support they may receive in their activities from relevant national or regional initiatives.

In this topic the integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement.

2.3.4.4 Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

Chapter	**FPP Phase**
Excellence	60 pages
Impact	100 pages
Quality and efficiency of the Implementation	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

2.3.4.5 Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Max Contribution per partner (% of the total EU funding): 40 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details).

Participation is limited to legal entities established in EU Member States, Norway, Iceland, and Israel (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

2.3.4.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

2.3.4.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.4.8 Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.4.9 Score

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Excellence	0-5	1.0	3
Impact	0-5	1.0	3
Quality and efficiency of the Implementation	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.3.4.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	**Maximum EU Contribution as % of the Eligible Cost according to HE (*)**
For profit organization but not an SME	50 %
SME (for profit SME)	50 %
University/Other (not for profit)	50 %

(*) beneficiaries may ask for a lower contribution.

Purchases of equipment or other assets used for the action must be declared as depreciation costs. However, costs may exceptionally be declared as full capitalised costs for high-value equipment that is essential for the development of the pilots, particularly where such equipment contributes to the development of an EU ecosystem of equipment providers and users, and ultimately to European technological autonomy. This exception may apply where the equipment represents a significant share of the beneficiary's eligible costs and where limiting the cost to depreciation would introduce delays in the implementation or compromise project objectives. The list of eligible items to be declared as full capitalised costs must be part of the proposal and will be confirmed by the Chips JU during the grant preparation process.

2.3.4.11 STEP and Sovereignty Seal

This topic contributes to the objectives of the *Strategic Technologies for Europe Platform* (STEP). As such, eligible proposals that exceed the evaluation thresholds will be awarded a *Sovereignty Seal*. The Sovereignty Seal is a quality label, valid for the duration of the project, which will facilitate access to additional EU funding (alternative, cumulative or combined funding from several EU budget instruments) or national public and private investments.

2.3.5 Supporting developing Quantum Chip Technology for neutral atoms stability Pilot

Topic: HORIZON-JU-Chips-2025-QAC1-5-SGA

Type of Action	RIA Specific grant agreement in relation to a Framework Partnership Agreement
Indicative EU budget	25 M€
Expected EU contribution per project	25 M€
GMode	Co-funded with the NFA One stage, with submission of Full Project Proposal (FPP)
Invitation date	30th July 2025
Deadline FPP	17th September 2025

2.3.5.1 Context

Within the Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots, the selected consortia will be invited to submit a proposal that will implement the first 3-4 years of the action plan for providing stable pilot fabrication capabilities defined in the FPA that would foster quantum chips production and rapid innovation tailored to meet the needs of the European quantum industry over the next decade, in particular start-ups and SMEs. The testing and experimentation facilities should be fully integrated in the pilots, providing seamless production and testing services.

2.3.5.2 Expected outcomes.

The proposal should aim to establish neutral atoms stability pilot production capabilities for a first of their kind quantum technology, where in the future European companies, research centres and academic institutions can produce quantum chips on a stable pilot scale based on a shared cost model between users and service providers. The targeted stability pilot should have a simple baseline process ready in 2-3 years from start of the project - reaching at least Technology Readiness Level (TRL) 6.

An early industrialization roadmap should be available by month 6 of the project, with the expectation that it will be regularly updated throughout the project’s lifetime to incorporate

evolving technical progress, market needs, and alignment with industrial partner requirements for scaling and commercialization towards mass production.

The proposal should focus on developing scalable production processes for quantum chips, with the goal of establishing industrial-level manufacturing methods. This includes the integration of cutting-edge Quantum Process Design Kits (PDKs) with the European Design Platform, aiming to standardize production workflows and minimize the need for custom developments. The proposal should include enabling technologies for quantum chips, namely advanced tools, components, and systems that facilitate the design, fabrication, operation, testing, and scaling of these devices. However, it should not include activities aimed at developing other essential components or subsystems that are unrelated or not directly integrated with the quantum chips. The initiative should seek to enhance technology and manufacturing readiness levels across the quantum industry, targeting applications in quantum computing, communications, simulations, and sensing. A key objective should be to establish standardized methodologies for the design, testing, and manufacturing of quantum chips, ensuring efficient production processes and broadening the range of applications in various sectors.

Key milestones should be clearly defined, with ambitious and technology-specific KPIs such as high yield, high-quality quantum chips, reliability, reproducibility, performance, and scalability of production. In addition, the proposal is expected to appropriately address the shortcomings identified in the Evaluation Summary Report of the corresponding FPA awarded under topic Chips-QAC-1, as appropriate to the relevant activities in the current SGA phase.

The proposal should demonstrate scalable, efficient, and stable production capabilities, with a focus on achieving high yield and consistency in quantum chip manufacturing. This will involve developing robust, repeatable manufacturing processes tailored to the unique requirements of neutral atoms quantum chips, ensuring a reliable supply chain for European stakeholders. Additionally, the proposal should outline the development of reliable characterization tools to ensure quality assurance, demonstrating the scalability of pilot technologies from small-to-mid volume fabrication to large-scale industrial production. A comprehensive technology roadmap and implementation plan should be defined to guide the industrialization of quantum chip production in the future and ensure the sustainability and growth of the quantum industry.

2.3.5.3 Scope

The action will require expertise in the area of manufacturing flows for quantum technologies, in particular in quantum computing/simulation (e.g. qubit fabrication), communication and sensing, and with issues regarding high-quality, reliability, versatility, process control including integrated testing and minimizing lead times. Interaction with standardisation bodies and data sharing on benchmarking is also encouraged.

The proposal should also cover: (i) the collaboration with other initiatives or programmes at regional, national, or European level such as Framework Partnership Agreements (FPAs) awarded under topic Chips-QAC-2: Call for establishing Framework Partnership Agreement(s)

for developing Quantum Chip Technology for high-quality Stability Pilots, and the relevant Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots. This includes synergies and cooperation with the experimental pilot lines QU-PILOT and QU-TEST of the Quantum Flagship Initiative, for R&D support; (ii) any additional financial support they may receive in their activities from relevant national or regional initiatives.

In this topic the integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement.

2.3.5.4 Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

Chapter	**FPP Phase**
Excellence	60 pages
Impact	100 pages
Quality and efficiency of the Implementation	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

2.3.5.5 Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Max Contribution per partner (% of the total EU funding): 40 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details).

Participation is limited to legal entities established in EU Member States, Norway, Iceland, and Israel (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

2.3.5.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

2.3.5.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.5.8 Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.5.9 Score

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Excellence	0-5	1.0	3
Impact	0-5	1.0	3
Quality and efficiency of the Implementation	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.3.5.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	Maximum EU Contribution as % of the Eligible Cost according to HE (*)
For profit organization but not an SME	50 %
SME (for profit SME)	50 %
University/Other (not for profit)	50 %

(*) beneficiaries may ask for a lower contribution.

Purchases of equipment or other assets used for the action must be declared as depreciation costs. However, costs may exceptionally be declared as full capitalised costs for high-value equipment that is essential for the development of the pilots, particularly where such equipment contributes to the development of an EU ecosystem of equipment providers and users, and ultimately to European technological autonomy. This exception may apply where the equipment represents a significant share of the beneficiary's eligible costs and where limiting the cost to depreciation would introduce delays in the implementation or compromise project objectives. The list of eligible items to be declared as full capitalised costs must be part of the proposal and will be confirmed by the Chips JU during the grant preparation process.

2.3.5.11 STEP and Sovereignty Seal

This topic contributes to the objectives of the *Strategic Technologies for Europe Platform* (STEP). As such, eligible proposals that exceed the evaluation thresholds will be awarded a *Sovereignty Seal*. The Sovereignty Seal is a quality label, valid for the duration of the project, which will facilitate access to additional EU funding (alternative, cumulative or combined funding from several EU budget instruments) or national public and private investments.

2.3.6 Supporting developing Quantum Chip Technology for high-quality Trapped Ions Pilot

Topic: HORIZON-JU-Chips-2025-QAC2-SGA

Type of Action	RIA Specific grant agreement in relation to a Framework Partnership Agreement
Indicative EU budget	25 M€
Expected EU contribution per project	25 M€
CMode	Co-funded with the NFA One stage, with submission of Full Project Proposal (FPP)
Invitation date	30th July 2025
Deadline FPP	17th September 2025

2.3.6.1 Context

Within the Framework Partnership Agreements (FPAs) awarded under topic Chips-QAC-2: Call for establishing Framework Partnership Agreements for developing Quantum Chip for high-quality Trapped Ions Pilots, the consortium is invited to submit a proposal that will implement the first 3-4 years of the action plan for providing high-quality pilot fabrication capabilities defined in the FPA that would foster trapped-ions quantum chips production and rapid innovation tailored to meet the needs of the European quantum industry over the next decade, in particular start-ups and SMEs. The testing and experimentation facilities should be fully integrated in the pilot, providing seamless production and testing services.

2.3.6.2 Expected outcomes.

The proposal should aim to establish stability pilot production capabilities for a first of their kind quantum technology, where in the future European companies, research centres and academic institutions can produce quantum chips on a stable pilot scale based on a shared cost model between users and service providers. The targeted trapped-ions pilot should have a simple baseline process ready in 2-3 years from start of the project - reaching at least Technology Readiness Level (TRL) 6.

An early industrialization roadmap should be available by month 6 of the project, with the expectation that it will be regularly updated throughout the project's lifetime to incorporate

evolving technical progress, market needs, and alignment with industrial partner requirements for scaling and commercialization towards mass production.

The proposal should aim to develop a robust European supply chain for trapped-ion quantum technologies covering the entire value chain from materials to applications, and enhancing their availability for computing, communication, and sensing applications. The proposal should also focus on encouraging innovation within SMEs and ensuring that critical intellectual property remains within the EU. The proposal should also demonstrate high-quality production processes, emphasizing the maturation of scalable and efficient manufacturing capabilities. The integration of Quantum Process Design Kits (PDKs) should be a key focus, ensuring that the production process is streamlined and adaptable, thus enhancing Europe's leadership in quantum technologies.

The proposal should include enabling technologies for quantum chips, namely advanced tools, components, and systems that facilitate the design, fabrication, operation, testing, and scaling of these devices. However, it should not include activities aimed at developing other essential components or subsystems that are unrelated or not directly integrated with the quantum chips. By fostering a community of interest in quantum technologies and enabling the use of cutting-edge trapped-ion chips, the project will significantly boost innovation capacity, providing a competitive advantage for the European ecosystem in the global market.

Key milestones should be clearly defined, with ambitious and trapped-ion-specific KPIs such as high yield, high-quality quantum chips, reliability, reproducibility, performance, and scalability of production. In addition, the proposal is expected to appropriately address the shortcomings identified in the Evaluation Summary Report of the corresponding FPA awarded under topic Chips-QAC-2, as appropriate to the relevant activities in the current SGA phase.

2.3.6.3 Scope

The action will require expertise in the area of manufacturing flows for trapped-ion quantum technologies, in particular in quantum computing/simulation (e.g. qubit fabrication), communication and sensing, and with issues regarding high-quality, reliability, versatility, process control including integrated testing and minimizing lead times. Interaction with standardisation bodies (e.g., for trap socket designs, modularity interfaces, or photonic integration) and data sharing on benchmarking is also encouraged.

The proposal should also cover: (i) the collaboration with other initiatives or programmes at regional, national, or European level such as the Framework Partnership Agreements (FPAs) awarded under topic Chips-QAC-1: *Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots*. This includes synergies and cooperation with the experimental pilot lines QU-PILOT and QU-TEST of the Quantum Flagship Initiative, for R&D support; (ii) any additional financial support they may receive in their activities from relevant national or regional initiatives.

In this topic the integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement.

2.3.6.4 Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

Chapter	**FPP Phase**
Excellence	60 pages
Impact	100 pages
Quality and efficiency of the Implementation	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

2.3.6.5 Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Max Contribution per partner (% of the total EU funding): 40 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details).

Participation is limited to legal entities established in EU Member States, Norway, Iceland, and Israel (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

2.3.6.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

2.3.6.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.6.8 Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.6.9 Score

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Excellence	0-5	1.0	3
Impact	0-5	1.0	3
Quality and efficiency of the Implementation	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.3.6.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	**Maximum EU Contribution as % of the Eligible Cost according to HE (*)**
For profit organization but not an SME	50 %
SME (for profit SME)	50 %

University/Other (not for profit)	50 %

(*) beneficiaries may ask for a lower contribution.

Purchases of equipment or other assets used for the action must be declared as depreciation costs. However, costs may exceptionally be declared as full capitalised costs for high-value equipment that is essential for the development of the pilots, particularly where such equipment contributes to the development of an EU ecosystem of equipment providers and users, and ultimately to European technological autonomy. This exception may apply where the equipment represents a significant share of the beneficiary's eligible costs and where limiting the cost to depreciation would introduce delays in the implementation or compromise project objectives. The list of eligible items to be declared as full capitalised costs must be part of the proposal and will be confirmed by the Chips JU during the grant preparation process.

2.3.6.11 STEP and Sovereignty Seal

This topic contributes to the objectives of the *Strategic Technologies for Europe Platform* (STEP). As such, eligible proposals that exceed the evaluation thresholds will be awarded a *Sovereignty Seal*. The Sovereignty Seal is a quality label, valid for the duration of the project, which will facilitate access to additional EU funding (alternative, cumulative or combined funding from several EU budget instruments) or national public and private investments.

2.4 Lab to Fab Accelerators Ecosystem

With its rapidly rising computing demands, Europe's vibrant industrial ecosystem needs new perspectives for a substantial growth potential. Using traditional monolithic SoCs, design and fabrication costs are increasing exponentially from one leading edge node to the next. Chiplets, instead, can be an efficient and economical way out providing the basis for a crucial push. Using chiplets in packaging architectures aims to reduce product costs while enabling the manufacture of new high-performance functionalities.

With their modular design, chiplet architectures allow the mix-and-match of various functional blocks, thus providing greater flexibility and making it easier to customise and upgrade computing components, driving scalability and adaptability. This way, they meet the demands of industrial sectors like high-performance computing, automotive, avionics, aerospace, communications, and secure & trustworthy electronics systems.

However, a successful integration of chiplets requires advanced heterogeneous integration techniques. Surpassing traditional methods like full-chip integration and 2.5D integration, they will pave the way for emerging innovative chiplet business models potentially reshaping market segments in the coming years. While the benefits of this evolution for the European economy appear to be obvious, the success of this transition will largely depend on targeted transfer activities from the lab into European fabs – for an optimised exploitation right from the pilot line to the industry.

To that end, the European Union is funding the establishment of European RTO-based pilot lines addressing innovative and advanced packaging technologies. Notably, the APECS pilot line, which unites leading research institutes across Europe in advanced packaging, the NanoIC pilot line offering advanced interconnect technologies, the FAMES pilot lines with new 3D integration options, as well as the PIXEurope and WBG pilot lines, which focus on the integration and packaging of photonic and high-power integrated circuits.

These pilot lines implemented under the EU Chips Act, will serve as key research providers for latest heterogeneous integration and advanced packaging technologies.

To achieve the effective incorporation of heterogeneously integrated and chiplet-based systems and establish a seamless pipeline from research to product development to pilot lines, Lab to Fab Transfer Accelerator (LFA) projects will be crucial for a rapid take-up of these technologies by European industry.

2.4.1 Lab to Fab Accelerators for Advanced Packaging and heterogeneous integration

Topic: DIGITAL-JU-Chips-2025-SG-LFA

Type of Action	Simple Grant
Indicative EU budget	50 M€
Expected EU contribution per project	The JU estimates that an EU contribution between EUR 12 and 16 million per project would allow to appropriately address the expected outcomes. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA One stage Call, with submission of Full Project Proposal (FPP)
Call launch date	3 December 2025
Deadline FPP	25 February 2026 at 17:00 Brussels Time

2.4.1.1 Context

The Lab-to-Fab Transfer Accelerator (LFA) projects prepare for a faster take-up of latest packaging technologies by the European industry. They do not cover the full lab-to-fab trajectory but prepare it and should enable a seamless fab technology transfer to industry after the end of the project.

2.4.1.2 Expected outcomes.

This topic will open up new opportunities for European-based semiconductor packaging companies and their supply chain by building on currently available services of RTOs and all Chips JU pilot lines. The LFA projects should prepare and speed up the transfer of technologies from pilot lines to industrial deployment.

In addition, projects should expand the advanced packaging ecosystem in Europe and boost its competitiveness by offering a fast path towards industrialization of European semiconductor technology.

Through possible involvement of appropriate actors across the value chain – from materials, substrate, equipment, and test providers through packaging companies and their European customers – proposed projects should build a strong European innovation and transfer

ecosystem for advanced packaging solutions, contributing to new and resilient supply chains in Europe.

Project proposals need to address several of the following expected outcomes:

- **Advanced packaging solutions tailored to European market needs** available for direct transfer into mass manufacturing within European production facilities (TRL 7) establishing a foundation for large-scale production in Europe for targeted application sectors.
- **Optimized utilization and demonstrable impact of Chips JU pilot lines**, accelerating development and validation of advanced packaging innovations.
- **Enhanced global competitiveness of European industry**, through increased capabilities in advanced packaging technologies (including chiplets), supporting faster adoption of cutting-edge semiconductor technologies in Europe.
- **Lowered economic and technical barriers for industrial capacity expansion**, through co-development enabling quicker adoption of heterogeneous integration and chiplet technologies in commercial products.
- **Strengthened investment confidence and market traction** for medium- to high-volume production by proving the readiness of technologies for qualified series manufacturing.
- **Alignment of advanced packaging capabilities in Europe with needs in strategic application areas**, including edge high-performance computing (eHPC), artificial intelligence (AI), power electronics, sensors, photonics, security, safety, and mobility.
- **Improved electronic system performance and energy efficiency**, achieved through integration of multichip, chiplet, and 3D technologies in high-demand applications such as eHPC, AI, and 5G.
- **Contribution to environmental sustainability and resource efficiency**, through advanced module and package designs that reduce material and energy usage in chip production.

2.4.1.3 Scope

To bring the latest advanced packaging technologies from the Chips JU pilot lines to industrial advanced packaging sites across Europe faster, the Chips Joint Undertaking will support **pan-European technology transfer preparation projects** to accelerate the post-project transfer from Chips JU pilot lines into key application domains.

The focus of the proposed projects should be on joint development, led by industry, of the most advanced packaging technologies with the Pilot lines to enable a future transfer of the latest packaging technologies from pilot lines into industrial production sites. The proposed projects are expected to cover the necessary value chain steps up to manufacturing, and develop industrial-grade, high-yield advanced packaging technologies including process developments up to TRL 7.

The proposed projects should define pathways into (one of) the following **two industrialization streams after the end of the projects**:

(1) Enabling an open-access heterogeneous integration and chiplet packaging **foundry** for European key applications;

(2) and/or **transfer of technologies** to companies for setting-up or upgrading own advanced packaging manufacturing lines **in Europe** for key European markets.

Proposal consortia should be led by industry and contain concrete deployment scenarios for one or both of those streams.

The proposed projects should address one or more of the following topics:

1) Special demands for **Communication Technologies** and **RF based applications**, e.g.
   - WLP and Fan-Out Wafer Level Packaging (FOWLP) with RDL for small and medium volume;
   - Efficient heterogeneous integration strategies of multiple material systems, e.g. Si, GaN, GaAs and 2D materials;
   - Special requirements of high frequency radars especially for the interconnection between the components and the substrate to guarantee the high performance of the whole system;
   - Other RF specific packaging needs not covered above.
2) Special demands for **Photonics applications**, e.g.
   - Optical Die-to-Die communication packaging solutions;
   - Co-packaging of photonics for known-good tested Photonic ICs;
   - Standardisation of optical die interface to facilitate automatic testing operations;
   - Efficient heterogeneous integration strategies of multiple material systems, e.g. Si, SOI, SiN, InP, and 2D materials;
   - Other photonics specific packaging needs not covered above.
3) Special demands for **HPC, edge-HPC and power delivery**, e.g.
   - Advanced and highly functional organic IC substrates with a 4× reduction in line/space and pad pitch, achieving feature dimensions comparable to those of silicon interposers and silicon bridges;
   - Introduction of novel materials, such as glass, for advanced IC substrates enabling enhanced functional integration, including embedded components;
   - Adherence to application-specific packaging guidelines, e.g. Large Package for HPC and AI (e.g. IC-substrate CTE and materials);
   - Integrated passive/active devices manufacturing in RDLs and substrates;
   - 3D interconnect methods including hybrid bonding;
   - Packaging and cooling of high-power-dissipating components/modules including smart power chips and PMICs (e.g. embedding);
   - Other HPC and edge-HPC specific packaging needs not covered above including integration of new functionalities, devices and packaging technologies.
4) Special demands for **Novel Sensor Applications**, e.g.

- Advanced packaging, 3D integration and WLP for sensors and actuators;
- Embedded active devices / components / novel sensor and actuator approaches (like TMR and others) in PCB/IC-substrate with chip(s) assembly co-design, leveraging the Design Platform capabilities;
- MEMS test and simulation including stress sensor for calibration and chip-package interaction and in-field compensation;
- Higher system integration level for ECUs and sensors/actuator modules:
  - Logic + Memory (computing/embedded HPC);
  - Logic + Power + Sensor + Actuator integration.
- Other novel sensors specific packaging needs not covered above.

5) Special demands for **automotive, and other harsh environment applications** (such as energy, industrial, avionics, aerospace, etc.), e.g.
   - Parts, materials and processes for extreme application (exceeding -55 / +125°C) such as GaN, SiC, Diamond related semiconductors;
   - Development of packaging and assembly procedures for very high temperature applications including high power and thermal control;
   - Assessment of new materials for very high radiation dose;
   - Development of new testing procedures for very extreme temperatures (i.e. sockets, thermal chambers, feedthrough connectors, etc.);
   - Other harsh environments specific packaging needs not covered above.

In addition, accelerator projects should enable a faster qualification and technology transfer of advanced packaging and heterogeneous chip integration technologies for uptake by European manufacturing sites. More specifically, the proposed projects should:

- **Address industrial requirements** for advanced heterogeneous integration and chiplet based future products regarding cost, performance, security and reliability standards.
- **Pave the way to manufacturability** by manufacturing-grade process developments and standardisation for scalability and cost competitiveness.
- **Include implementation Roadmap**: Proposals should provide an implementation roadmap for enabling Chips Act related first-of-a-kind investments in Europe that address industrialisation and technology expectations beyond the project's duration and capacity.
- **Design for built-in testability**, i.e. cooperation with chiplet designers to ensure that chiplets will be accessible for testing by Automatic Test Equipment.
- **Enhance faster industrial technology qualification schemes and adaptation** with qualification plans for appropriate verticals with suitable reliability tests for market and mission profile, enabling fast track to industrial deployment.
- **Apply "System Technology Co-Optimization" (STCO)**, address increased modularity and reusability of design blocks and enhance standardized integration technologies based on PDKs (process design kits) and ADKs (assembly design kits) for the heterogeneous chiplet packaging.
- **Address EDA verification**, i.e. design rule checks, process design checks.

- **Utilize advanced materials**, e.g. advanced substrates including organic but also inorganic ones, i.e. glass technologies.

All projects selected from this call are expected to contribute actively to the CSA, under the topic DIGITAL-Chips-2025-CSA-LFA, that will support the projects selected under this topic and that will coordinate core efforts to ensure a coherent ecosystem development, standardisation tasks and cross-sectional technology exchange to create maximum synergies.

2.4.1.4 Admissibility

Admissibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Regarding page limits:

Chapter	FPP Phase
Relevance	60 pages
Implementation + chapter 4 of the template for the proposal (Part B)	100 pages
Impact	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

2.4.1.5 Eligibility

Eligibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Specific eligibility conditions:

Size limit	15 participants
Max EU Contribution per partner (% of the total EU funding)	50%

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to participation restrictions for the protection of European digital infrastructures, communication and information systems, and related supply chains, as described in Annex 4 of the WP General Annexes.

Legal entities that are established in the Union or EEA countries but are controlled from third countries may only participate on the condition that they guarantee the protection of the essential security interests of the Union and the Member States and that they ensure the protection of classified documents information. Where applicable, security guarantees need to be provided after proposal selection.

2.4.1.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

2.4.1.7 Evaluation procedure

For the specificity of each call evaluation please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

For the priority order of proposals with the same score, please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

2.4.1.8 Award criteria.

Please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Specific rules may apply regarding the eligibility to national funding.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.4.1.9 Score

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Relevance	0-5	1.0	3
Implementation + chapter 4 of the template for the proposal (Part B)	0-5	1.0	3
Impact	0-5	1.5	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.4.1.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to DIGITAL.

Type of beneficiary	EU Contribution as % of the Eligible Cost according to DIGITAL (*)
For profit organization but not an SME	25 %
SME (for profit SME)	35 %
University/Other (not for profit)	35 %

(*) beneficiaries may ask for a lower contribution.

2.4.2 Lab to Fab Accelerator ecosystem - Coordination and Support Actions. Boosting cooperation for industrial implementation on advanced packaging of chiplets and heterogeneous integration in Europe.

Topic: DIGITAL-JU-Chips-2025-CSA-LFA

Type of Action	Coordination and Support Actions (CSA)
Indicative EU budget	2 M€
Expected EU contribution per project	The JU estimates that an EU contribution of around EUR 2 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amount.
Mode	EU funding only One stage Call with submission of Full Project Proposal (FPP)
Call launch date	03 December 2025
Deadline FPP	25 February 2026 at 17:00 Brussels Time

2.4.2.1 Context

This coordination and support action will support the Lab to Fab Transfer Accelerator (LFA) projects to leverage synergies and standardisation efforts, maximising the efficiency of joint deployment and speeding up future transfer into industrial applications. It will help to close gaps in advanced packaging capabilities in Europe and contribute to building a stronger European ecosystem.

Therefore, this CSA is intended to effectively support the **selected projects under Call DIGITAL-JU-Chips-2025-SG-LFA**.

2.4.2.2 Expected outcomes.

This CSA is expected to deliver a more resilient, sustainable, and competitive European advanced packaging ecosystem through focused collaboration, standardization, and workforce development.

The following outcomes are expected:

1. Resilient & Diversified Supply Chains (Addressing Supply Network Ecosystems)

A demonstrably more resilient European supply chain for advanced packaging, evidenced by a publicly available vulnerability assessment for key sectors (automotive, aerospace, healthcare, security, telecommunications).

2. Sustainable & Resource-Efficient Manufacturing

Reduced environmental footprint of advanced packaging manufacturing in Europe, demonstrated by measurable improvements in resource consumption (materials, energy) and adoption of sustainable design principles.

3. Accelerated Standardization & Interoperability

Increased adoption of standardized technologies for advanced packaging, fostering interoperability and reducing time-to-market for European companies.

4. Enhanced Collaboration & Knowledge Sharing

A strengthened and interconnected European advanced packaging ecosystem, characterized by increased collaboration between research institutions, industry, pilot lines, competence centres, and existing networks (e.g. Pack4EU).

5. Coordinated R&I & Industrial Implementation

A harmonized roadmap for the industrial implementation of research results in advanced packaging, ensuring coherence between EU R&I activities and industry needs.

6. Skilled & Competent Workforce

A skilled workforce equipped to support the growth of the European advanced packaging ecosystem, with increased availability of specialized training programs and upskilling opportunities.

2.4.2.3 Scope

The CSA should address, but is not limited to, the following areas:

Enable **collaboration and exchange**:

- Provide coordination on common objectives and coordinated dissemination between the projects of the LFA programme,
- Disseminate to and between lab-to-fab projects best practices in “System Technology Co-Optimization” (STCO) and support building STCO ecosystems at project level,
- Organise networking and collaboration of stakeholders from the EU with a view to addressing current needs, considering future requirements and stimulating long-term cooperation,
- Connect with and leverage services by competence centres to derive training material and platform information, serving competence centres, pilot lines and the design platform,
- Foster the exchange of achievements in Process Design Kit (PDK) and Assembly Design Kit (ADK) for the heterogeneous chiplet packaging, and the EDA verification.

Identifying, mapping and disseminating of **standardisation** results:

- Support standardised integration technologies based on PDKs (process design kits) and ADKs (assembly design kits), complementing the offering of the Pilot lines' PDKs,
- Monitor manufacturing-grade process developments and standardisation for scalability and cost competitiveness,
- Track heterogeneous package integration schemes that are customisable and flexible, to enable diversified advanced packaging building blocks for European markets,
- Collect and disseminate the project results on standardised or exchangeable interfaces for all packaging layers, e.g. for chiplet and other advanced semiconductor-based components,
- Foster and report on intelligent leveraging and developing technological standards to provide credible cost-down pathways and competitive time-to-market.

Identify and support **roadmap activities and synergies**:

- Organise and support roadmap activities
    - through networks, conferences, workshops and other actions that support semiconductor joint EU R&I activities,
    - by generating R&I priorities for potential future collaboration,
    - by connecting EU companies in the semiconductor value chain to exchange information and propose measures to improve chip supply chain stability.
- Support exchange of researchers and closer coordination of running R&I activities which address equal or similar objectivities to leverage synergies,
- The action should ensure that relevant stakeholders from the EU are engaged during the process through regional and international workshops and a set of communication and dissemination actions.

Reminding that of general importance to the Chips JU calls are:

- Re-use of results from previous ECSEL JU, Chips JU, H2020, HE or EUREKA-cluster projects on the Packaging topic is encouraged. Of particular importance the CSA is expected to build up on the results of the Pack4EU CSA.
- Developing synergies with other relevant European, national or regional initiatives and/or funding programmes on the Packaging topic.
- Collaboration with industrial associations in the field (e.g. with EPoSS and AENEAS) and specialized clusters. Collaboration with associations of microelectronic assembly and packaging science.
- In particular, paying attention to the needs of SMEs, involving SMEs, start-ups and scale-ups in project execution, and develop solutions that can be taken up and/or exploited by SMEs.

To ensure proper coordination and support to the LFA programme, the CSA is expected to have a 4-year duration.

2.4.2.4 Admissibility

Admissibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Regarding page limits:

Chapter	FPP Phase
Relevance	20 pages
Implementation + chapter 4 of the template for the proposal (Part B)	60 pages
Impact	20 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

2.4.2.5 Eligibility

Eligibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Specific eligibility conditions:

Size limit	15 participants
Max EU Contribution per partner (% of the total EU funding)	50%

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to participation restrictions for the protection of European digital infrastructures, communication and information systems, and related supply chains, as described in Annex 4 of the WP General Annexes.

Legal entities that are established in the Union or EEA countries but are controlled from third countries may only participate on the condition that they guarantee the protection of the essential security interests of the Union and the Member States and that they ensure the protection of classified documents information. Where applicable, security guarantees need to be provided after proposal selection.

2.4.2.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

2.4.2.7 Evaluation procedure

For the specificity of each call evaluation please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

For the priority order of proposals with the same score, please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

2.4.2.8 Award criteria.

Please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Specific rules may apply regarding the eligibility to national funding.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.4.2.9 Score

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Relevance	0-5	1.0	3
Implementation + chapter 4 of the template for the proposal (Part B)	0-5	1.0	3
Impact	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.4.2.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to DIGITAL.

Type of beneficiary	EU Contribution as % of the Eligible Cost according to DIGITAL (*)
For profit organization but not an SME	100 %
SME (for profit SME)	100 %

University/Other (not for profit)	100 %

(*) beneficiaries may ask for a lower contribution.